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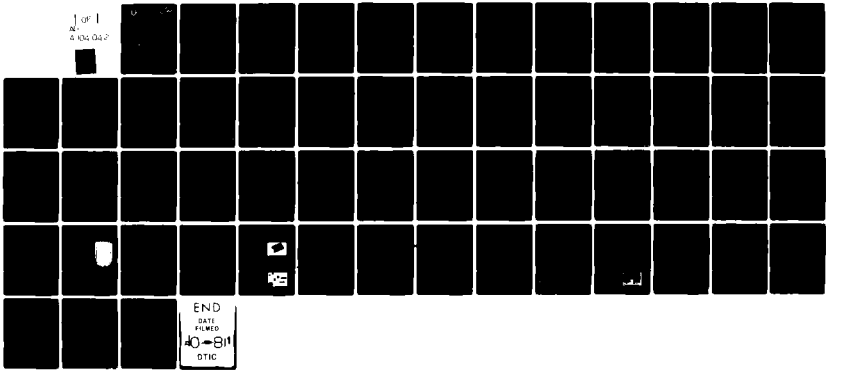

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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

J.E. Brewer and J.W. Dzimianski

WESTINGHOUSE ELECTRIC CORPORATION
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Baltimore, Maryland 21203

Aug 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A manufacturing methods project has been initiated to establish production techniques for 8K-bit metal-nitride-oxide semiconductor (MNOS) block-oriented random-access memory (BORAM) devices, to establish the performance adequacy and reproducibility of such MNOS BORAM devices for military environments, and to demonstrate a production rate of 500 multicuip MNOS BORAM hybrid circuits per month. During the past reporting period the project has focused on definition of tests, development

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of test equipment, and preparation of test programs. In particular, studies have been conducted to determine the feasibility of using an automated retention projection (RP) test as part of a manufacturing screen.

TABLE OF CONTENTS

Page

1. NARRATIVE AND DATA 1-1

   1.1 CONCEPTS AND OBJECTIVES 1-1
   - 1.1.1 Integrated Screening Approach 1-1
   - 1.1.2 Retention Projection Concept 1-3
   - 1.1.3 RP Test Implementation 1-3

   1.2 RETENTION PROJECTION TEST CHARACTERISTICS 1-9
   - 1.2.1 RP Test Parameters 1-9
   - 1.2.2 Sources of Variability 1-10
   - 1.2.3 Repeatability Experiment 1-12
   - 1.2.4 Estimate of Precision 1-12

   1.3 MNOS BORAM DEVICE OBSERVATIONS 1-12
   - 1.3.1 Parameters of Interest 1-18
   - 1.3.2 Nominal Condition Distribution 1-18
   - 1.3.3 Temperature Effects 1-18
   - 1.3.4 Erase-Write Time Effects 1-25
   - 1.3.5 Endurance Effects 1-28

2. CONCLUSIONS 2-1

3. PROGRAM FOR NEXT INTERVAL 3-1

4. PUBLICATIONS AND REPORTS 4-1

5. DEVICE DATA SHEET 5-1

6. DISTRIBUTION LIST 6-1

LIST OF ILLUSTRATIONS

Figure		Page
1-1	Simplified Data Storage and Readout Sequence	1-4
1-2	Retention Projection Program Simplified Flow Diagram	1-5
1-3	Minimum Write Voltage Search Subroutine	1-6
1-4	Voltage Sweep Subroutine	1-7
1-5	BORAM Chip Retention Projection	1-8
1-6	Post Burn-In Minimum Write Voltage Histogram	1-20
1-7	Post Burn-In Slope Histogram	1-22
1-8	Temperature Trend Plots for Eight Samples	1-24
1-9	Erase-Write Cycles vs Minimum Write Voltage (Unbalanced Stress)	1-30
1-10	Erase-Write Cycles vs Slope (Unbalanced Stress)	1-31
1-11	Retention Projection vs Erase-Write Cycles	1-32

LIST OF TABLES

Table		Page
1-1	Repeatability Data for RP Test	1-13
1-2	Repeatability Data for RP Test	1-14
1-3	Repeatability Data for RP Test	1-15
1-4	Repeatability Data for RP Test	1-16
1-5	Repeatability Data for RP Test	1-17
1-6	Repeatability Data for RP Test	1-17
1-7	Post Burn-In Minimum Write Voltages	1-19
1-8	Post Burn-In Slope	1-21
1-9	Temperature Test Data for Eight Samples	1-23
1-10	RP Test Results for Varied Pulsewidths	1-25
1-11	ANOVA for Erase and Write Time Effects on Minimum Voltage	1-26
1-12	ANOVA for Erase and Write Time Effects on Slope	1-27
1-13	ANOVA for Erase and Write Time Effects on Log (Time) Projection	1-27
1-14	Minimum Write Voltage vs Erase-Write Cycles	1-28
1-15	Slope vs Erase-Write Cycles	1-29

1. NARRATIVE AND DATA

The feasibility of a nondestructive quick response screen for retention and endurance characteristics is under investigation. Specifically, tests suitable for use with MNOS BORAM devices as manufactured at Westinghouse are being considered. The approach taken is called "Retention Projection," and the term "RP" test is used below as a short notation.

This report outlines study objectives, presents preliminary results concerning the nature of the RP test, and provides some data and speculations on observed device RP characteristics under different conditions.

It should be made clear at the outset that the RP test does not provide a highly accurate, verifiable, estimate of retention time. The scheme projects short time retention observed at low-write voltages to an expected retention at nominal write voltage. For typical devices ready to be shipped, the projected times exceed 10^9 hours or more than 10^5 years. Numbers of this magnitude cannot be verified readily by human beings. Repeated RP tests show decades of variation in the projected time, so high precision cannot be claimed. The value expected from the test is limited to providing a general indicator or figure of merit sensitive to endurance-retention related device characteristics.

At the current stage of development, the RP test approach shows some promise of being useful as the basis for a screen to remove defective or suspect devices from the population. Some form of an RP test is visualized as being part of a comprehensive set of stresses and tests oriented toward endurance-retention phenomena.

1.1 CONCEPTS AND OBJECTIVES

The advent of nonvolatile semiconductor memory requires that methods be developed to predict device retention and endurance within a few seconds of test time. This investigation has focused on one approach to achievement of that goal, i.e., the Retention Projection or RP test. It is to be stressed that an RP test is viewed as only one part of a suitable device screen. Further, the value of the RP test lies in the prediction of device quality. It is not expected to be a numerically accurate predictor of retention.

This discussion will set forth an overall device screening approach, the RP concept, and finally will outline a specific experimental implementation of an RP test. (The BORAM device is described in the data sheet included under Section 5.)

1.1.1 Integrated Screening Approach

MNOS BORAM parts are used in a wide variety of applications where reliable operation in hostile environments is essential. Observation of individual devices and experience with similar parts indicates that the technology is capable of providing desired reliability and performance. Devices free from inherent material defects and manufacturing induced defects will perform properly.

The objective of screening during manufacture is to detect and eliminate parts which contain defects. Toward this end, the body of practice defined in Mil-M-38510 and Mil-Std-883 apply directly to MNOS BORAM.

Because MNOS BORAM offers nonvolatile data retention, the basic screening approach must be expanded. Retention is known to be a function of accumulated erase-write cycles, and this so-called "endurance" phenomena must be considered. Screens must incorporate application of stresses which will excite retention-endurance oriented failure modes, and must introduce tests which are sensitive to retention-endurance anomalies.

The primary stresses currently employed in the BORAM screen are "cycle stress" and "burn-in." After assembly, every BORAM multichip hybrid package (MHP) is subjected to 2500 erase-write cycles using a checkerboard data pattern, and then 2500 cycles using the complement of the checkerboard data pattern. The purpose of this stress is to cause defective memory cells to progress noticeably toward failure. In a similar scheme, each MHP is subjected to more than 160 hours of 125°C burn-in while operating in the read mode.

To detect endurance-retention related defects, several different kinds of tests are being used in combination. The types of tests include erase-recovery tests, low-voltage write tests, and short time observation of retention. The specific groups of tests used are somewhat experimental, and are expected to be modified as experience with the product grows.

The erase-recovery (ER) tests are intended to detect poor pulse response of memory transistors. The scheme is to erase-write the complement of a data pattern ten times, and then erase-write and read the data pattern one time. For this sequence to work properly the transistor in each two-transistor cell that was subjected to eleven erase pulses, must recover in response to one write pulse. To test the other half of each cell, the ER sequence must be repeated complementing the initial data patterns.

Low-voltage write tests are an attempt to eliminate parts which are suspect because they tend to differ from the bulk of the device population. The use of low-write voltage is somewhat related to the RP test scheme, but is relatively crude in discrimination capability. The sequence is to erase the part using nominal supply voltage, write the part using some fixed but reduced supply voltage, wait a specified time, and then read the part at nominal supply voltage.

With low-write voltage the amount of charge stored in the memory transistors is reduced, and retention times can be shortened to seconds. At present, each MHP is tested using 26 volts from VCC to VGG during write with a 2-second delay before reading.

Experiments have shown that for two seconds read delay the bulk of the MNOS BORAM population operates at write voltages on the order of 19 to 25 volts. Parts as high as 26 volts form the upper tail of the distribution. During the hybrid assembly and test sequence, the low-voltage write test is applied before and after stress applications. If a device endurance-retention related defect is excited, it is hypothesized that the 2-second reduced write-voltage characteristic will be affected. Thus the arbitrary cut-off limit of 26 volts will eliminate such parts.

In the absence of a "fool proof" quick response test, some short time observations of data retention are currently being used. Attempts to observe actual retention are useful in that very weak parts can be identified. Obviously, real-time observations cannot be said to be an adequate screen because of the necessary time restrictions.

Several forms of real-time retention tests have been used. The conditions have been a matter of equipment convenience. Parts were required to retain a checkerboard pattern for 16 hours when stored without power at 80°C. The same parts were then required to retain a complement checkerboard pattern for 16 hours at 80°C.

The burn-in stress has also provided a convenient opportunity for a retention test. In this case, the zero data pattern is written into the device before burn-in. During the 125°C stress the part is operated in the read mode. After removal and cool down (under power) the parts are read to verify data retention.

1.1.2 Retention Projection Concept

Measurements performed on small quantities of MNOS BORAM 6008 devices showed that the logarithm of retention time (tr) varied linearly with the supply voltage present during the write operation (Vw). The observed relationship was:

$$\log (tr) = m\,Vw + b$$

The slope (m) is measured in decades per volt. Retention time (tr) is in hours, and the voltage during write (Vw) is in volts. The intercept is of course expressed as the logarithm of hours.

The straight line can readily be shown to hold over a small range of voltage where the corresponding retention times are small. The RP concept assumes that the relationship will hold when the write voltage is increased to nominal levels. Thus the slope and intercept parameters of the straight line can be defined using several low voltage measurements, and the pseudo retention at nominal voltage can be computed.

1.1.3 RP Test Implementation

Over a period of several months, experimental trials were conducted to establish an automated RP test which was suitable for conducting investigations into product characteristics and screening approaches. Figures 1-1 to 1-4 document the essential features of that implementation.

The heart of the approach is the data storage and data readout subroutine shown in figure 1-1. In the data storage routine the complement of the desired pattern is first stored using the nominal 30-volt condition. The purpose of this operation is to provide a repeatable starting point for the low-voltage test. The chip is then erased, and the voltage is set to the desired reduced value. A real-time clock is started in order to measure retention time, and the writing operation is initiated. Some time later the data readout subroutine will be entered. At that time the real-time clock will be read, and the device data will be readout.

Figure 1-2 shows the overall flow of the RP test. The program finds the reduced voltage (minV) at which the part will retain data for about 0.5 second. The details of the search procedure for minV are given in figure 1-3. The program then conducts a sweep of four additional voltage points differing from minV by increments of 50 millivolts. At each voltage a real-time measurement of retention is performed. Figure 1-4 presents the voltage sweep subroutine. After the measurements are complete, the program converts the time measurements to log time and performs a least squares fit of the data to a straight line. Various tabulations, plots or reports are then prepared depending on operator requests. Figure 1-5 is an example of the plotted results from an RP test on a BORAM 6008 device.

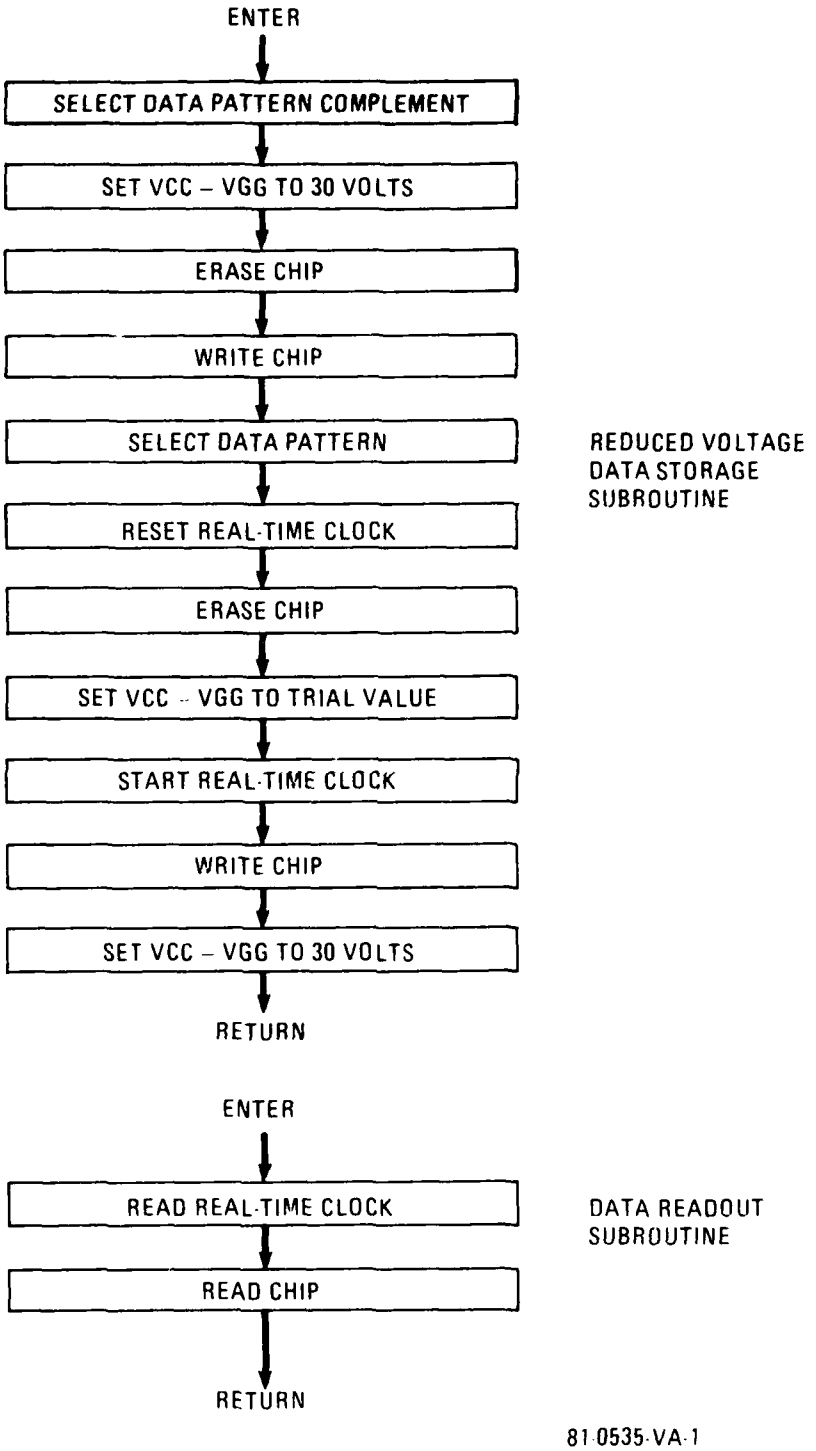


Figure 1-1. Simplified Data Storage and Readout Sequence

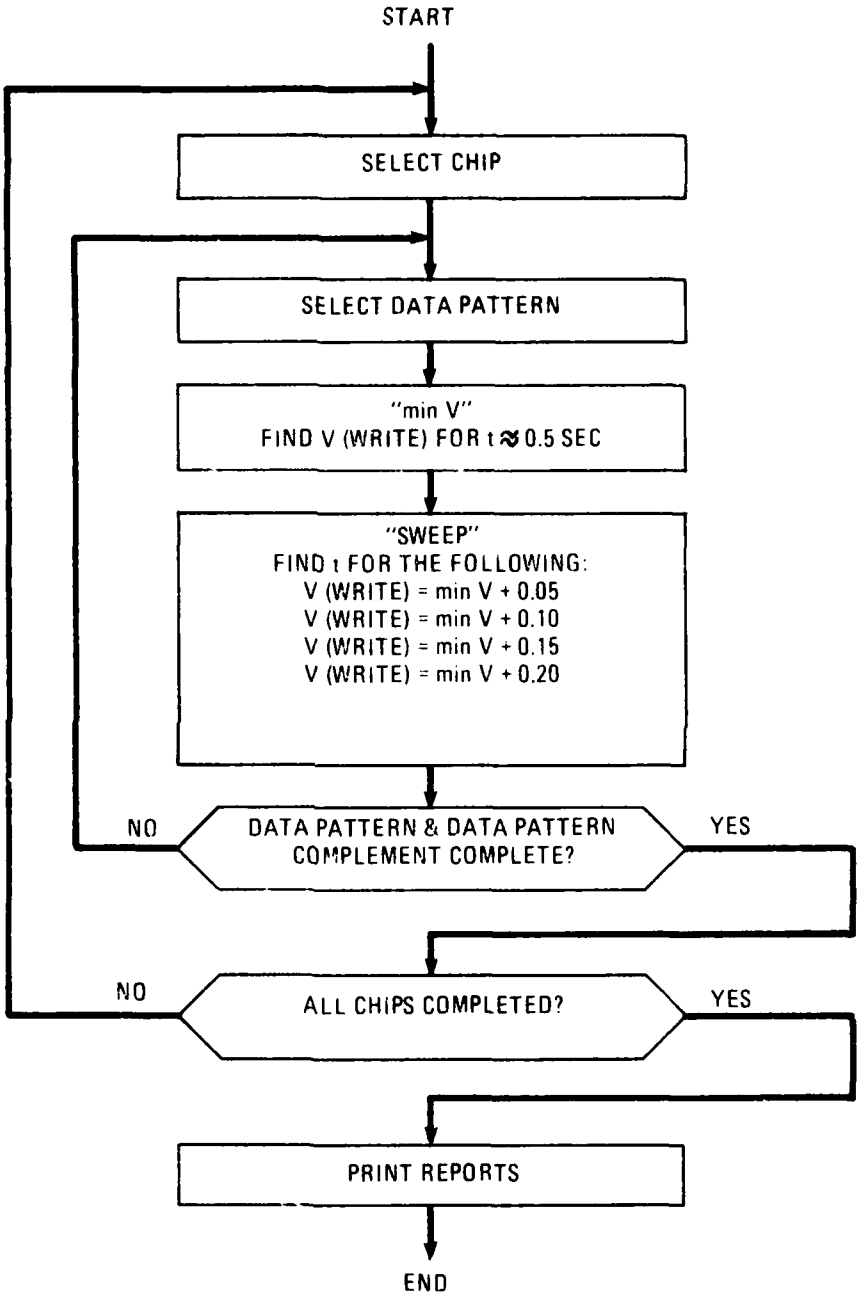


Figure 1-2. Retention Projection Program Simplified Flow Diagram

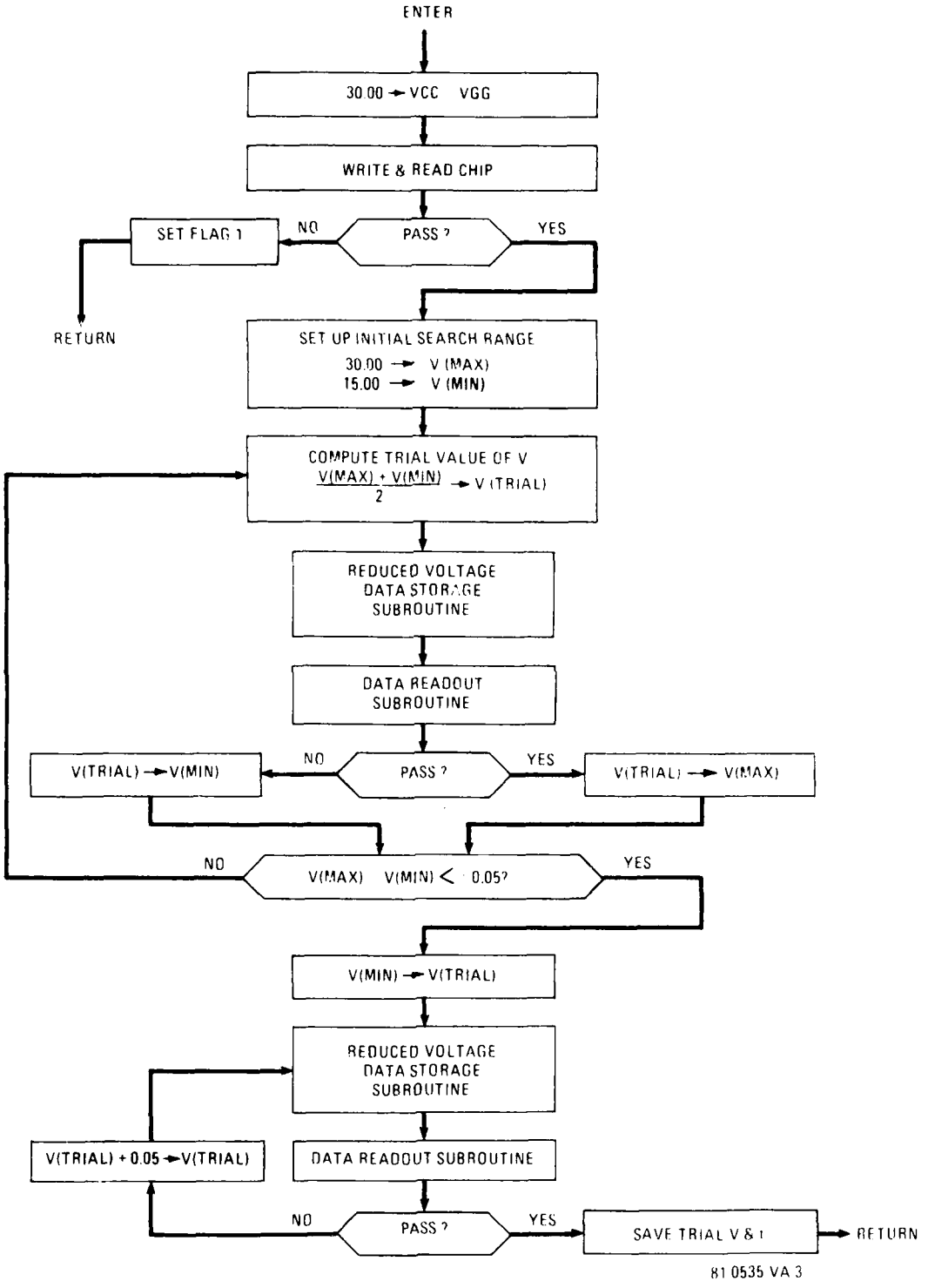


Figure 1-3. Minimum Write Voltage Search Subroutine

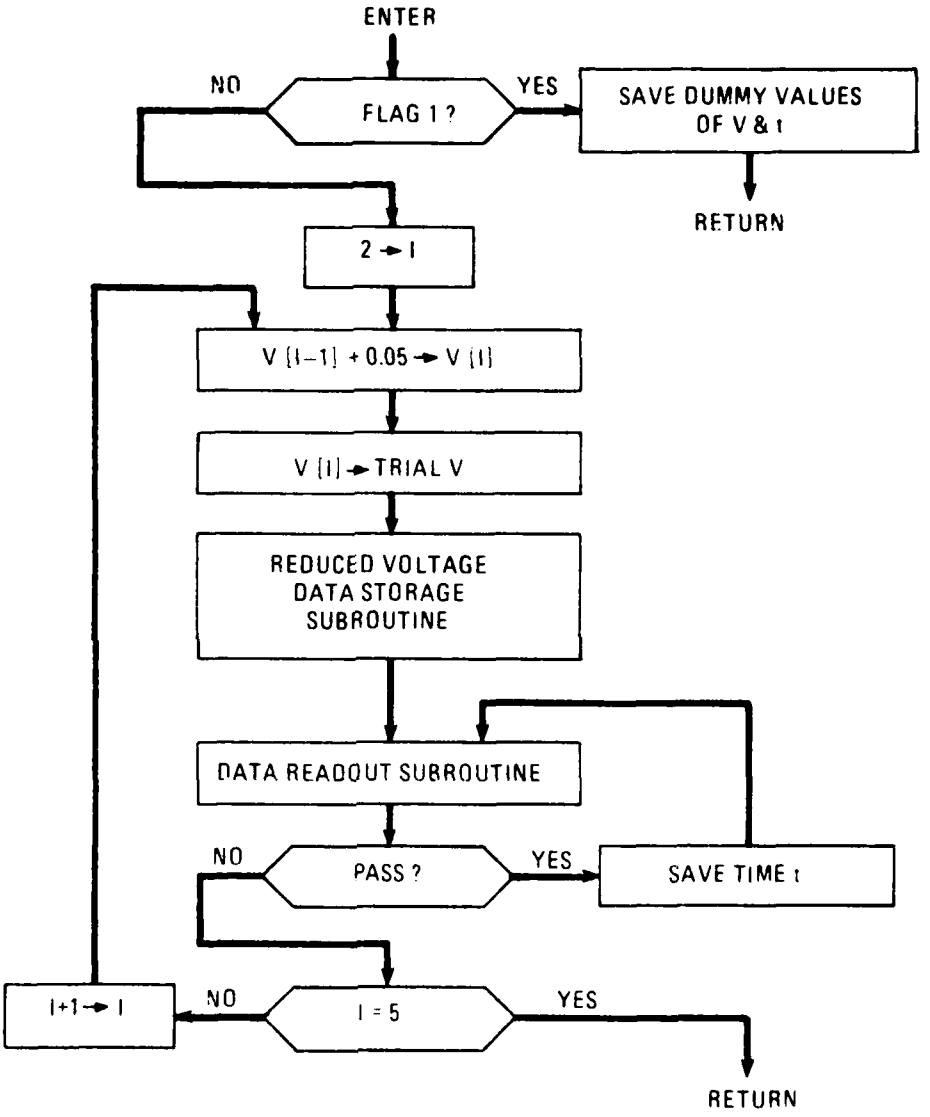
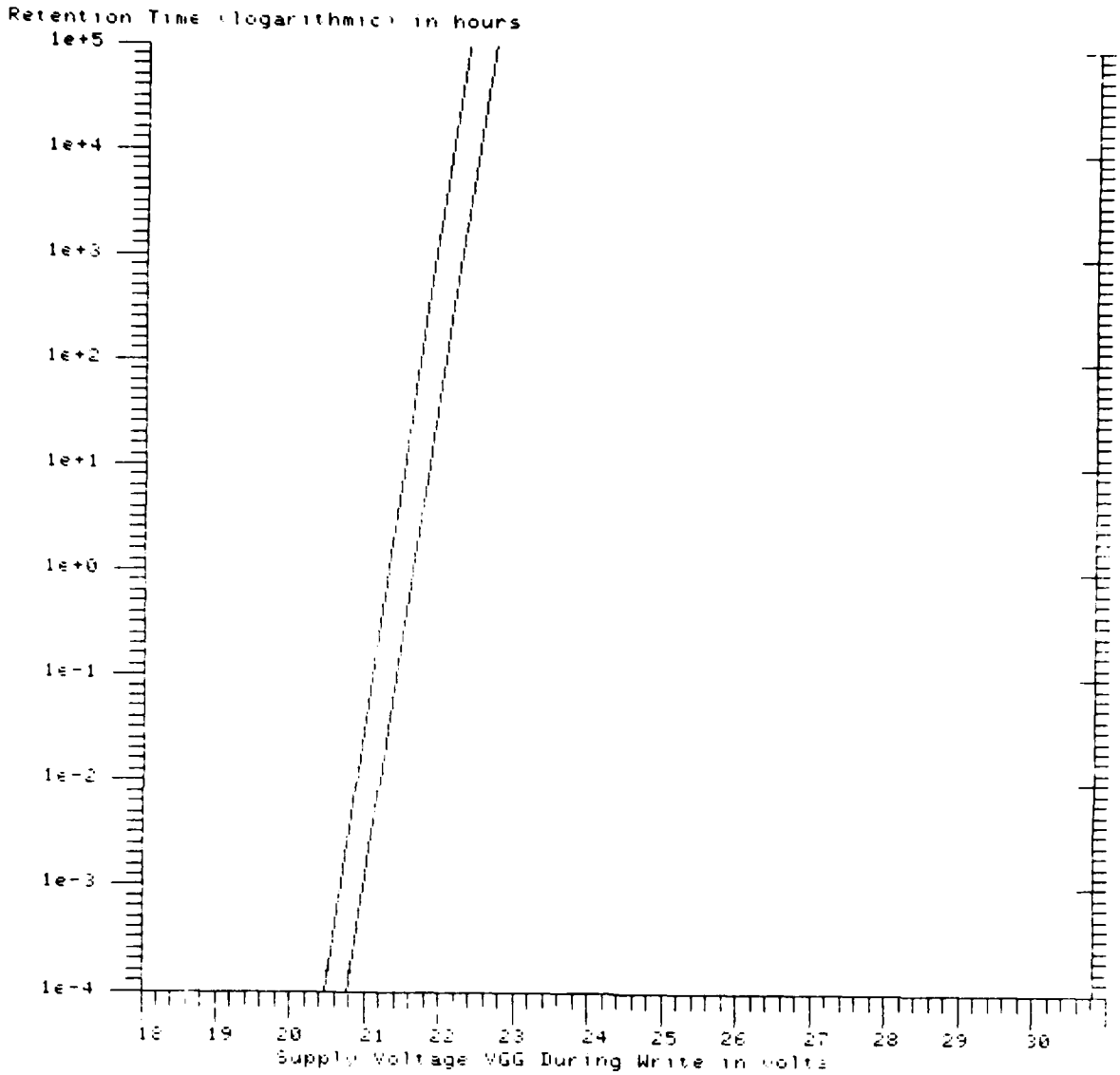


Figure 1-4. Voltage Sweep Subroutine



BORAM Chip Serial#101 19 MAY 81
Erase: Chip Mode Erase Write Times 1000 200 microseconds

#	CHBD Pattern VGG	CHBD Pattern Hours			CHBD EAP Pattern VGG	CHBD EAP Pattern Hours
1	20.80	1.55E-04			20.50	1.55E-04
2	20.85	2.36E-04	4.7095	.....slope..... 4.8703	20.55	2.35E-04
3	20.90	3.93E-04	5.33E-101	...intercept... 4.91E-103	20.60	3.93E-04
4	20.95	7.11E-04	0.9967	...corr.coef... 0.9956	20.65	7.43E-04
5	21.00	1.35E-03			20.70	1.44E-03

Projected Hours=3.054E 39 Projected Hours=2.618E 42

Projected Years=3.484E 35 Projected Years=2.987E 38

81-0535-VA-5

Figure 1-5. BORAM Chip Retention Projection

1.2 RETENTION PROJECTION TEST CHARACTERISTICS

The RP concept can be implemented in many different ways. To be useful the test results must be shown to be reproducible, and to be related to the product characteristics in a meaningful way. This discussion will review some of the considerations involved in defining the details of the RP test, and will present the results of some repeatability experiments.

1.2.1 RP Test Parameters

In simplified form the RP test consists of data storage under reduced supply voltage conditions, and observation of the stored data until a data failure is observed. This process must be repeated until sufficient voltage and time points have been established to allow a projection of the retention time at nominal supply voltage.

As a starting point for consideration of the elements of an RP test, a simplified model of a memory cell and of the behavior of the individual memory transistors will be reviewed.

A drain source protected (DSP) MNOS BORAM memory transistor operates by the electronic transfer of charge into and out of the gate insulator. Application of a positive gate voltage results in the threshold voltage being shifted in a positive direction. This is the erased condition or erased state. Application of a negative voltage causes a negative threshold shift, and the device is said to be in the written state.

After being written, the threshold voltage can be observed to decay in a positive direction. For a defect free device to a first order model, the threshold voltage changes as a linear function of the logarithm of the elapsed time after writing for times of interest in BORAM applications.

For an erased device, the threshold voltage will decay in a negative direction. For nominal BORAM operating conditions, the transistor threshold voltage immediately after erase will be determined primarily by the nonmemory portion of the drain source protected transistor. Only a very slight decay will be observed. After an elapsed time on the order of one hour the memory portion of the DSP transistor will dominate the decay. To a first order model, the threshold will be observed to change as a linear function of the logarithm of time where the slope in volts per decade of time is greater than the slope for times less than one hour.

A simplified concept of reading a two-transistor memory cell is that of a sense amplifier comparing the threshold voltages of the two memory transistors. As long as the threshold voltage difference is greater than the minimum discrimination voltage of the sense amplifier, the data can be reliably readout. One transistor is decaying from the erased state, and the other transistor is decaying from the written state.

It is convenient to speak of the difference between the threshold voltages as being the "window." The window voltage plotted against the logarithm of elapsed time tends to exhibit linear segments. At short times the decay or window closure rate is determined primarily by the written transistor. After about one hour the closure rate is affected by both transistors.

The initial window and the rate of decay is affected by the voltages and pulsewidths used for erase and for write. The two transistors are not necessarily decaying toward the same end-point threshold.

A bit of reflection on the various aspects of this simplified model will lead to an obvious conclusion. It is not possible to use a reduced voltage erase and/or write and simulate the "normal" end of retention condition. The DSP structure, and the dependence of decay rates on voltage levels, will not allow the short time (seconds) reduced voltage conditions to duplicate the long time (years) nominal voltage conditions.

It follows then that predictions of retention time based on low-voltage observations cannot reasonably be expected to coincide with actual nominal voltage real-time retention. On the other hand, the low-voltage predicted retention is derived from the memory cell operation under a specific set of conditions, and should be related in some manner to real-time retention. Thus it is reasonable to expect that projected retention may be a useful figure of merit.

A retention projection test thus need not attempt to simulate any particular aspect of nominal cell operation. It simply must be based on a repeatable scheme. A convenient arrangement is to use a nominal supply voltage during erase and a reduced supply voltage during write. The erase condition will make it easier to establish a reproducible initial condition.

Test time is an important consideration. The fastest time can be achieved if the first reduced write voltage point is taken at the shortest read delay time the test system can resolve. For the initial RP test implementation that time was 559 milliseconds.

Again, test time will be minimized if additional data points are taken as close to the initial 559-millisecond point as possible. Because of the characteristics of the programmable power supply used to provide the voltage, the smallest possible increment is 0.05 volt.

The simple-minded model of the memory cell given above can be used to visualize the RP test situation. A sense amplifier acts to compare the threshold voltages of the two-memory transistor which form the cell. One transistor is in the erased state as a consequence of having been erased using nominal operating voltages. The other transistor has been moved slightly in the direction of the written state by operating in the write mode with reduced supply voltage.

The sense amplifier is in effect comparing the nonmemory threshold of the erased memory transistor with the written transistor threshold. Thus the write voltage to achieve any given fixed retention time (e.g., 2 seconds) will be a function of the nonmemory threshold.

1.2.2 Sources of Variability

The premise of the RP test is a relationship between retention time t and the supply voltage during write V. The most obvious implications of this relationship for variation in test results will be examined, and the most common sources of experimental error will be identified.

Using a simplified notation, the basic equation is of the form:

$$\log t = A + B V$$

$$t = a10^{BV} \quad (\text{where } a = 10^{A})$$

The partial derivatives of interest would be:

$$\frac{\partial \log t}{\partial V} = \frac{\partial}{\partial V}(A + BV) = B$$

$$\frac{\partial t}{\partial V} = \frac{\partial}{\partial V} a10^{BV} = Ba10^{BV} = Bt$$

Error in t resulting from error in V would be expressed as:

$$\Delta \log t = \left[\frac{\partial}{\partial V}(\log t)\right]\Delta V = B\Delta V$$

$$\Delta t = \left[\frac{\partial t}{\partial V}\right]\Delta V = Bt\Delta V$$

$$\frac{\Delta t}{t} = B\Delta V$$

Errors in V are amplified by the slope factor B in the computation of log t. The resulting error in t is even greater, and is proportional to Bt.

Looking at the relationship from the point of view of attempting to estimate the equation, errors in V are more important than errors in t.

The experimental situation during the RP test consists of two parts. First, five data points are established where voltage and retention are observed. Second, that data is used to compute a slope in decades per volt and a retention projection in hours.

The primary uncertainty in measured time values results from the amount of time required to write and read the 256 addresses in the BORAM 6008 chip. Ideally, the read delay time should be related to single memory cells. It should be the time from the end of cell write to the time when the sense amplifier sets up. In practice, single cells cannot be conveniently distinguished.

The RP test allows the operator to enter write pulsewidth into the control computer before initiating a run. Given a 200-microsecond write pulse, the chip write time would be about 60 milliseconds. Chip read time is about 10 milliseconds. Thus from the viewpoint of individual cell read delay times, a difference of 50 milliseconds exists from address 0 to address 255.

Time is measured by a real-time clock associated with the control computer. Readout resolution is one millisecond. The clock is started at the beginning of the write operation, and is readout at the beginning of the read operation.

The first data point is taken at a clock time of about 559 milliseconds. This time is accurate for the first address. For address 255 the actual delay time would be about 509 milliseconds, or about 9 percent lower.

The fixed 50-millisecond uncertainty would also be present for the next four data points. In these cases the read delay time would be larger, and the percentage uncertainty would be reduced for each succeeding point.

Supply voltages during write are not measured. Voltages are set by the computer via software commands. The resolution of the programmable power supply on the required range is 50 millivolts.

To establish the first data point, a search procedure is used to find the voltage on a 50-millivolt increment which just allows data to be retained for 559 milliseconds. Thus the uncertainty in the first voltage point is approximately 50 millivolts.

The criterion for the first data point is that the device holds data for more than 559 milliseconds. The 50-millivolt resolution causes an uncertainty in time as well as voltage. For a typical slope of three decades per volt and a nominal time of 0.56 second, the time uncertainty approaches $B\Delta Vt = 3 \times 0.05 \times 0.56 = 0.084$ second.

Additional error enters into the voltage because of line drops between the supply and the device under test. The impact of this source of error depends on how many devices are being tested and how the devices are connected. When long cables are used to reach devices located in temperature chambers this matter must be given careful consideration.

For data points number two to five, the voltage can be considered to be fixed and the time is the quantity to be measured. In this case, the 50-millivolt resolution of the supply does not introduce error.

In summary, it would seem that the primary source of variability in an RP test would be deviations in supply voltage. It is most likely that line drops between the programmable supply and the device under test will be the major problem.

1.2.3 Repeatability Experiment

For an RP test to be useful it must be shown to be repeatable. Two different experiments have been performed to examine this issue. This discussion will first describe the two experimental approaches, and then will discuss each set of observations.

1.2.3.1 Description of Experiments

The approach taken in both experiments was simply to execute the automated RP test several times for a given set of samples. Selected measured and computed quantities were then examined for repeatability by computing a number of elementary statistics.

One test employed two sample devices which were subjected to the RP test 50 times. Since each device was measured using two data patterns, four sets of data were obtained. Tables 1-1 to 1-4 summarize this information. The entire test sequence and data collection was automated. The control computer was programmed to execute the test 50 times, and to store the resulting data on a disc file. After the test was complete, additional programs were employed to prepare data summaries.

The other experiment employed six sample devices that were tested six different times. Tests were initiated manually over a period of a few days. Tables 1-5 and 1-6 give a partial summary of the results.

1.2.4 Estimate of Precision

For the present version of an RP test there are three parameters of immediate interest: the minimum write voltage, the slope, and the retention projection.

The definition of the minimum write voltage is limited by the power supply resolution of 50 millivolts. It appears that the short time repeatability of a minV measurement is ±50 mV. Over a period of several days this interval can expand to ±100 mV.

The slope measured in decades per volt exhibits a standard deviation that is on the order of 0.2 to 0.4 for short time repeatability. Over a period of several days the standard deviation can grow to about 0.5. It is perhaps more meaningful to speak in terms of the coefficient of variation (standard deviation divided by the mean). The short run coefficient is about 9 percent, and over a period of days it grows to about 10 percent.

The retention projection can of course vary broadly. Coefficients of variation for the log of time were 9.2, 8.1, 11.1, and 8.8 percent for the cases given in tables 1-1 to 1-4. Thus the variability of log t is on the order of 10 percent. The variability of t however depends on the magniltude of the mean value for t. At high mean values of t, a 10 percent deviation for log t can mean a change of two decades for t.

1.3 MNOS BORAM DEVICE OBSERVATIONS

The utility of the RP test depends on how sensitive it is to conditions within a device. A series of exploratory tests have been started to examine this issue. Data reported here is very preliminary, and has served primarily as a learning vehicle to allow formulation of more complete investigations.

Table 1-1. Repeatability Data for RP Test

BORAM 6008 Chip Serial #1001 — 19 MAY 81
Checkerboard Pattern, Erase Chip Mode, Erase/Write 1000/200 microseconds

Trial Number	Write Voltage Minimum	Delay Time (msec)	Slope decades per volt	Correlation Coefficient	Projected Petention log(t)	Projected Petention hours
01	21.35	559	2.8052	0.9991	20.450312	2.820E 20
02	21.35	559	2.7287	0.9993	19.784703	6.091E 19
03	21.35	559	2.4933	0.9993	17.757061	5.716E 17
04	21.35	559	2.3962	0.9995	16.914434	8.212E 16
05	21.40	559	2.9589	0.9945	21.667984	4.656E 21
06	21.35	559	2.4093	0.9964	17.011820	1.028E 17
07	21.40	559	2.8956	0.9974	21.112776	1.297E 21
08	21.40	559	2.7447	0.9915	19.831494	6.784E 19
09	21.40	559	2.8494	0.9978	20.713280	5.167E 20
10	21.40	559	2.7119	0.9926	19.545051	3.508E 19
11	21.40	559	2.7368	0.9970	19.747963	5.597E 19
12	21.40	559	2.6854	0.9963	19.308222	2.033E 19
13	21.40	559	2.6360	0.9954	18.885760	7.687E 18
14	21.40	559	2.5838	0.9952	18.434973	2.723E 18
15	21.40	559	2.6007	0.9946	18.582085	3.820E 18
16	21.40	559	2.6970	0.9975	19.398566	2.504E 19
17	21.40	559	2.6088	0.9989	18.638134	4.346E 18
18	21.40	559	2.5576	0.9986	18.195505	1.569E 18
19	21.40	559	2.5560	0.9980	18.186791	1.537E 18
20	21.40	559	2.4675	0.9987	17.423498	2.652E 17
21	21.40	559	2.5203	0.9991	17.875137	7.501E 17
22	21.40	559	2.4294	0.9976	17.090393	1.231E 17
23	21.40	559	2.4648	0.9971	17.405043	2.541E 17
24	21.40	559	2.4103	0.9977	16.934592	8.602E 16
25	21.40	559	2.4082	0.9976	16.916517	8.251E 16
26	21.40	559	2.4669	0.9987	17.418090	2.619E 17
27	21.40	559	2.4357	0.9990	17.140130	1.381E 17
28	21.40	559	2.3715	0.9981	16.600307	3.984E 16
29	21.40	559	2.3725	0.9981	16.609031	4.065E 16
30	21.40	559	2.3701	0.9977	16.583809	3.835E 16
31	21.40	559	2.3495	0.9959	16.414191	2.595E 16
32	21.40	559	2.3708	0.9981	16.594482	3.931E 16
33	21.40	559	2.3358	1.0000	16.278392	1.898E 16
34	21.40	559	2.3759	0.9994	16.623220	4.200E 16
35	21.40	559	2.3757	0.9994	16.622264	4.190E 16
36	21.40	559	2.2738	0.9972	15.757977	5.728E 15
37	21.40	559	2.3379	1.0000	16.296450	1.979E 16
38	21.40	559	2.2757	0.9998	15.764269	5.811E 15
39	21.40	559	2.2764	0.9998	15.770362	5.893E 15
40	21.40	559	2.3366	1.0000	16.285345	1.929E 16
41	21.40	559	2.2752	0.9998	15.760374	5.759E 15
42	21.40	559	2.3380	1.0000	16.297502	1.984E 16
43	21.40	559	2.3391	1.0000	16.306438	2.025E 16
44	21.40	559	2.2778	0.9998	15.782975	6.067E 15
45	21.40	559	2.2757	0.9984	15.758941	5.740E 15
46	21.40	559	2.3380	1.0000	16.297502	1.984E 16
47	21.40	559	2.3174	0.9983	16.123374	1.329E 16
48	21.40	559	2.2342	0.9991	15.407796	2.557E 15
49	21.40	559	2.2745	0.9998	15.754281	5.679E 15
50	21.40	559	2.3780	0.9994	16.641188	4.377E 16
mean.....	21.395	559.0	2.4746	0.9980	17.494016	
std deviation.....	0.015	0.0	0.1856	0.0019	1.610024	
coef of variation.	0.001	0.0	0.0750	0.0019	0.092033	
coef of skewness..	-2.558	0.0	0.8662	-1.4233	0.857679	
coef of kurtosis..	-18.971	$$$$$$	2.6879	8.8584	2.665467	

81-0535-TA-6

Table 1-2. Repeatability Data for RP Test

BORAM 6008 Chip Serial #1001 — 19 MAY 81
Checkerboard Bar Pattern, Erase Chip Mode, Erase/Write 1000/200 microseconds

Trial Number	Write Voltage Minimum	Delay Time (msec)	Slope decades per volt	Correlation Coefficient	Projected Retention log(t)	Projected Retention hours
01	20.50	559	2.8458	0.9997	23.227255	1.688E 23
02	20.50	558	2.6815	0.9997	21.661549	4.587E 21
03	20.55	559	3.1972	0.9939	26.439922	2.754E 26
04	20.55	559	3.1822	0.9963	26.289156	1.946E 26
05	20.55	559	3.0744	0.9945	25.274894	1.883E 25
06	20.55	559	3.0024	0.9952	24.592630	3.914E 24
07	20.55	559	2.9850	0.9964	24.418635	2.622E 24
08	20.55	558	2.8404	0.9942	23.059515	1.147E 23
09	20.55	559	2.9257	0.9972	23.858411	7.218E 23
10	20.55	559	2.8293	0.9971	22.943034	8.771E 22
11	20.55	559	2.7699	0.9973	22.387127	2.439E 22
12	20.55	559	2.7142	0.9976	21.850613	7.089E 21
13	20.55	559	2.6961	0.9992	21.678089	4.765E 21
14	20.55	559	2.7476	0.9997	22.161756	1.451E 22
15	20.55	559	2.7286	0.9986	21.971987	9.375E 21
16	20.55	559	2.6264	0.9986	21.014499	1.034E 21
17	20.55	559	2.6425	0.9995	21.155939	1.432E 21
18	20.55	559	2.5734	0.9991	20.516330	3.283E 20
19	20.55	559	2.5866	0.9996	20.630402	4.270E 20
20	20.55	559	2.5876	0.9996	20.639477	4.360E 20
21	20.55	559	2.5475	0.9988	20.256377	1.805E 20
22	20.55	559	2.4921	0.9993	19.740636	5.503E 19
23	20.55	559	2.3965	0.9995	18.834453	6.831E 18
24	20.55	559	2.4928	0.9995	19.741923	5.520E 19
25	20.55	559	2.3950	0.9995	18.820458	6.614E 18
26	20.55	559	2.4688	0.9965	19.503839	3.190E 19
27	20.60	559	2.9153	0.9936	23.627277	4.239E 23
28	20.60	559	2.9138	0.9935	23.613451	4.106E 23
29	20.55	559	2.4079	0.9964	18.926004	8.433E 18
30	20.55	559	2.4671	0.9956	19.482228	3.035E 19
31	20.55	559	2.3668	0.9961	18.537768	3.450E 18
32	20.60	559	2.8834	0.9929	23.327780	2.127E 23
33	20.60	559	2.8961	0.9975	23.433920	2.716E 23
34	20.60	559	2.8682	0.9939	23.183659	1.526E 23
35	20.60	559	2.8945	0.9975	23.418873	2.623E 23
36	20.60	559	2.8161	0.9881	22.703856	5.057E 22
37	20.60	559	2.7926	0.9930	22.474724	2.983E 22
38	20.60	559	2.8491	0.9978	22.990176	9.776E 22
39	20.60	559	2.8494	0.9978	22.992685	9.833E 22
40	20.60	559	2.7701	0.9974	22.250183	1.779E 22
41	20.60	559	2.7948	0.9930	22.495388	3.129E 22
42	20.60	559	2.7721	0.9954	22.273137	1.876E 22
43	20.60	559	2.8499	0.9966	23.002102	1.005E 23
44	20.60	559	2.8171	0.9979	22.689910	4.897E 22
45	20.60	559	2.7381	0.9969	21.949550	8.903E 21
46	20.60	559	2.8179	0.9979	22.697635	4.985E 22
47	20.60	559	2.8035	0.9953	22.568796	3.705E 22
48	20.60	559	2.7132	0.9912	21.731365	5.387E 21
49	20.60	559	2.8497	0.9966	23.000365	1.001E 23
50	20.60	559	2.7131	0.9913	21.729616	5.366E 21
mean.....	20.569	559.0	2.7518	0.9966	22.155387	
std deviation.....	0.028	0.2	0.1930	0.0026	1.815877	
coef of variation.	0.001	0.0	0.0701	0.0027	0.081961	
coef of skewness..	-0.184	-4.6	-0.0975	-0.9066	0.042046	
coef of kurtosis..	6.171	0.0	2.7448	3.4587	2.838843	

81-0535-TA-7

Table 1-3. Repeatability Data for RP Test

BORAM 6008 Chip Serial #1002 — 19 MAY 81
Checkerboard Pattern, Erase Chip Mode, Erase/Write 1000/200 microseconds

Trial Number	Write Voltage Minimum	Delay Time (msec)	Slope decades per volt	Correlation Coefficient	Projected Retention log(t)	Projected Retention hours
01	20.80	559	4.4355	0.9975	36.969737	9.327E 36
02	20.80	559	4.1596	0.9960	34.423904	2.654E 34
03	20.80	559	4.0305	0.9966	33.240211	1.739E 33
04	20.85	559	4.8155	0.9998	40.262941	1.832E 40
05	20.85	559	4.7286	0.9989	39.478588	3.010E 39
06	20.85	559	4.6634	0.9996	38.873899	7.480E 38
07	20.85	559	4.5842	0.9994	38.152414	1.420E 38
08	20.85	559	4.4944	0.9999	37.319212	2.086E 37
09	20.85	559	4.4520	0.9999	36.931875	8.548E 36
10	20.85	559	4.4730	0.9999	37.123715	1.330E 37
11	20.85	559	4.4410	0.9999	36.819874	6.605E 36
12	20.85	559	4.2962	0.9998	35.509124	3.229E 35
13	20.85	559	4.3047	0.9999	35.574368	3.753E 35
14	20.85	559	4.3294	0.9999	35.799484	6.302E 35
15	20.85	559	4.1844	1.0000	34.478606	3.010E 34
16	20.85	559	4.1608	0.9999	34.262457	1.830E 34
17	20.85	559	4.2347	1.0000	34.936240	8.635E 34
18	20.85	559	4.0883	0.9999	33.598697	3.969E 33
19	20.85	559	3.9363	0.9993	32.208161	1.615E 32
20	20.85	559	3.9155	0.9991	32.005715	1.013E 32
21	20.85	559	3.9904	0.9997	32.693309	4.935E 32
22	20.85	559	3.9596	0.9998	32.413271	2.590E 32
23	20.85	559	3.8775	0.9996	31.661074	4.582E 31
24	20.85	559	3.9326	0.9972	32.146775	1.402E 32
25	20.85	559	3.8915	0.9977	31.772751	5.926E 31
26	20.85	559	3.7931	0.9998	30.891886	7.796E 30
27	20.85	559	3.7666	0.9987	30.636541	4.331E 30
28	20.85	559	3.7974	0.9985	30.916722	8.255E 30
29	20.85	559	3.7975	0.9974	30.913773	8.199E 30
30	20.85	559	3.7399	0.9987	30.392029	2.466E 30
31	20.85	559	3.7137	0.9984	30.152191	1.420E 30
32	20.85	559	3.6812	0.9980	29.852630	7.122E 29
33	20.85	559	3.6805	0.9987	29.850526	7.088E 29
34	20.85	559	3.6458	0.9984	29.530446	3.392E 29
35	20.85	559	3.5880	0.9985	29.003288	1.008E 29
36	20.85	559	3.6824	0.9980	29.863036	7.295E 29
37	20.85	559	3.6479	0.9984	29.549543	3.544E 29
38	20.85	559	3.5541	0.9988	28.694087	4.944E 28
39	20.85	559	3.4896	0.9977	28.102436	1.266E 28
40	20.85	559	3.5251	0.9984	28.429734	2.690E 28
41	20.85	559	3.5547	0.9988	28.699714	5.009E 28
42	20.85	559	3.5271	0.9983	28.447435	2.802E 28
43	20.85	559	3.5578	0.9959	28.712549	5.159E 28
44	20.85	559	3.5205	0.9963	28.373592	2.364E 28
45	20.85	559	3.4544	0.9982	27.781283	6.043E 27
46	20.85	559	3.5206	0.9978	28.385766	2.431E 28
47	20.85	559	3.5571	0.9959	28.706884	5.092E 28
48	20.85	559	3.4925	0.9977	28.128003	1.343E 28
49	20.85	559	3.4560	0.9992	27.800452	6.316E 27
50	20.85	559	3.4547	0.9992	27.788807	6.149E 27
mean.....	20.847	559.0	3.9316	0.9987	32.165195	
std deviation.....	0.012	0.0	0.3897	0.0012	3.584924	
coef of variation.	0.001	0.0	0.0991	0.0012	0.111454	
coef of skewness..	-3.593	0.0	0.5740	-0.7619	0.569146	
coef of kurtosis..	96.615	######	2.0982	5.1138	2.082879	

81-0535-TA-8

Table 1-4. Repeatability Data for RP Test

BORAM 6008 Chip Serial #1002 — 19 MAY 81
Checkerboard Bar Pattern, Erase Chip Mode, Erase/Write 1000/200 microseconds

Trial Number	Write Voltage Minimum	Delay Time (msec)	Slope decades per volt	Correlation Coefficient	Projected Retention log(t)	Projected Retention hours
01	20.55	559	5.4202	0.9998	47.403751	2.534E 47
02	20.55	558	5.2400	0.9999	45.705437	5.075E 45
03	20.55	559	5.0268	0.9998	43.685068	4.842E 43
04	20.55	559	5.0266	0.9998	43.682532	4.814E 43
05	20.55	559	4.9234	0.9996	42.707403	5.098E 42
06	20.55	559	4.7460	0.9993	41.027501	1.065E 41
07	20.55	559	4.6724	0.9994	40.329810	2.137E 40
08	20.55	559	4.5318	0.9992	39.005245	1.012E 39
09	20.55	559	4.5101	0.9991	38.797277	6.270E 38
10	20.55	559	4.5625	0.9986	39.283105	1.919E 39
11	20.55	559	4.3351	0.9967	37.142969	1.390E 37
12	20.55	559	4.2935	0.9985	36.742938	5.533E 36
13	20.55	559	4.2739	0.9983	36.557892	3.613E 36
14	20.55	559	4.2497	0.9975	36.326439	2.121E 36
15	20.55	559	4.2120	0.9953	35.956486	9.047E 35
16	20.55	559	4.2088	0.9970	35.931955	8.550E 35
17	20.55	559	4.1612	0.9971	35.482969	3.041E 35
18	20.55	559	4.0305	0.9966	34.247897	1.770E 34
19	20.55	559	3.9201	0.9974	33.209045	1.618E 33
20	20.55	559	3.9196	0.9960	33.200845	1.588E 33
21	20.60	559	4.8488	0.9994	41.782053	6.054E 41
22	20.55	559	3.8423	0.9930	32.457251	2.866E 32
23	20.55	559	3.7784	0.9940	31.856752	7.190E 31
24	20.60	559	4.6856	0.9996	40.244537	1.756E 40
25	20.55	559	3.7841	0.9931	31.908878	8.107E 31
26	20.60	559	4.7342	0.9999	40.691477	4.914E 40
27	20.60	559	4.6819	0.9995	40.213652	1.636E 40
28	20.55	559	3.6860	0.9947	30.986940	9.704E 30
29	20.60	559	4.6939	0.9999	40.314568	2.063E 40
30	20.60	559	4.6159	1.0000	39.583713	3.835E 39
31	20.60	559	4.5501	0.9994	38.971338	9.361E 38
32	20.60	559	4.5847	0.9995	39.299925	1.995E 39
33	20.60	559	4.5114	0.9997	38.605513	4.032E 38
34	20.60	559	4.5989	0.9999	39.420323	2.632E 39
35	20.60	559	4.4929	0.9999	38.429084	2.686E 38
36	20.60	559	4.4733	0.9999	38.245516	1.760E 38
37	20.60	559	4.4546	0.9998	38.066429	1.165E 38
38	20.60	559	4.4122	0.9997	37.662311	4.595E 37
39	20.60	559	4.4837	0.9997	38.333247	2.154E 38
40	20.60	559	4.3224	0.9998	36.828920	6.744E 36
41	20.60	559	4.4168	0.9999	37.704496	5.064E 37
42	20.60	559	4.3224	0.9998	36.828336	6.735E 36
43	20.60	559	4.3206	0.9996	36.814342	6.521E 36
44	20.60	559	4.3412	0.9998	37.005549	1.013E 37
45	20.60	559	4.3952	0.9997	37.499061	3.155E 37
46	20.60	559	4.3053	0.9999	36.656387	4.533E 36
47	20.60	559	4.3457	0.9997	37.039607	1.095E 37
48	20.60	559	4.2815	1.0000	36.434135	2.717E 36
49	20.60	559	4.2807	1.0000	36.425954	2.667E 36
50	20.60	559	4.2773	0.9998	36.395819	2.486E 36
mean.....	20.576	559.0	4.4357	0.9987	37.982654	
std deviation.....	0.025	0.1	0.3550	0.0019	3.349657	
coef of variation.	0.001	0.0	0.0800	0.0019	0.088189	
coef of skewness..	-0.075	-6.4	0.2683	-1.6514	0.340837	
coef of kurtosis..	7.400	0.0	3.4167	3.1534	3.490897	

81-0535-TA-9

Table 1-5. Repeatability Data for RP Test

TRIAL NUMBER	WRITE VOLTAGE MINIMUM (VOLTS)					
	DEVICE 1	DEVICE 2	DEVICE 3	DEVICE 4	DEVICE 5	DEVICE 6
1	22.65	21.95	22.25	24.75	23.55	25.55
2	22.65	21.95	22.20	24.75	23.65	25.60
3	22.65	21.95	22.20	24.75	23.70	25.65
4	22.65	21.95	22.25	24.75	23.65	25.55
5	22.65	21.95	22.25	24.80	23.70	25.65
6	22.65	21.95	22.20	24.80	23.70	25.70
MEAN	22.65	21.95	22.23	24.77	23.66	25.62
STD DEVIATION	0.00	0.00	0.03	0.03	0.06	0.06
COEF OF VARIATION %	0.00	0.00	0.13	0.12	0.25	0.23
COEF OF SKEWNESS	–	–	-0.00	0.55	-0.88	0.04
COEF OF KURTOSIS	–	–	-7.11	0.00	2.06	0.74

81-0535-TA-16

Table 1-6. Repeatability Data for RP Test

TRIAL NUMBER	COMPUTED SLOPE (DECADES PER VOLTS)					
	DEVICE 1	DEVICE 2	DEVICE 3	DEVICE 4	DEVICE 5	DEVICE 6
1	5.4616	3.6171	6.3666	3.0174	1.8791	2.1725
2	5.8175	3.5470	5.5047	2.8456	1.9476	1.8744
3	6.0778	3.6456	5.5072	2.6619	1.8726	1.7451
4	5.3582	3.2061	6.3395	2.6425	2.0623	2.0634
5	5.5339	3.1870	6.3727	2.9155	1.9504	2.2099
6	5.8143	3.2314	5.4339	2.8177	1.9954	1.8274
MEAN	5.6772	3.4057	5.9208	2.8168	1.9512	1.9821
STD DEVIATION	0.2712	0.2192	0.4816	0.1450	0.0717	0.1931
COEF OF VARIATION %	4.7770	6.4363	8.1340	5.1477	3.6747	9.7422
COEF OF SKEWNESS	0.2021	0.0375	-0.0057	0.0031	0.2692	0.0229
COEF OF KURTOSIS	1.2149	0.7583	0.7046	1.2102	1.3974	0.9484

81-0535-TA-17

1.3.1 Parameters of Interest

The minimum write voltage (0.5-second retention), the slope, and the retention projection are the major RP test parameters. The purpose of these exploratory tests is to learn about these parameters in two different ways. First, what is the natural distribution of each parameter for product in process? Distribution data is essential to planning intelligent screens. Second, how do the RP parameters change when a device is subjected to temperature, to varied erase and/or write timing, and to erase-write cycling.

In these first tests the emphasis has been on the mechanics involved. Gross issues of test adequacy and data interpretation were the primary focus.

1.3.2 Nominal Condition Distribution

Acceptance tests which may include some variation of an RP test should consider the natural distribution of the RP parameters for product which is ready for delivery.

A population of nine BORAM multichip hybrid packages (MHP) were subjected to the RP test. These devices had completed the cycle stress and burn-in required before delivery.

Table 1-7 lists the minimum write voltages observed for the 144 chips in the nine MHP's. Because checkerboard and checkerboard bar observations were required, a total of 288 write voltages were measured. Figure 1-6 gives a histogram of the results, and lists the basic statistics of the population.

Slope data was treated in a similar fashion in table 1-8 and figure 1-7. Use of the RP test gave some new information concerning these particular parts. The existence of the distribution tails was previously unknown. Follow-up investigations are planned to see if the behavior of the extreme devices is deficient.

1.3.3 Temperature Effects

In an attempt to explore the nature of RP characteristics over the temperature range, a set of eight sample devices were evaluated. Table 1-9 presents the major parameters for −55°C, 25°C, and 125°C. Data for the checkerboard pattern was plotted in figure 1-8 to see if any visual trends existed.

A trend toward longer projected retention at higher temperatures seems to exist. Individual devices do not always follow the trend, so some questions exist. The normal change of threshold voltage with temperature would cause a shift in the minimum write voltage in the direction shown. But the observed magnitude of change is greater than can be accounted for by this mechanism alone.

The devices were connected to the test system through relatively long cables. The error in write voltage because of the cables is a function of cable resistance and of the current demand of the devices under test. The current drawn by a BORAM device varies considerably with temperature. It appears that further work should be done to evaluate the "cable effect" before temperature test results are interpreted.

Table 1-7. Post Burn-In Minimum Write Voltages

HYBRID CIRCUIT SERIAL	PATTERN	POST BURN-IN MINIMUM WRITE VOLTAGE (VOLTS)															
		CHIP 1	CHIP 2	CHIP 3	CHIP 4	CHIP 5	CHIP 6	CHIP 7	CHIP 8	CHIP 9	CHIP 10	CHIP 11	CHIP 12	CHIP 13	CHIP 14	CHIP 15	CHIP 16
202	CKBD	26.30	22.20	19.80	19.15	18.75	19.75	19.50	20.40	19.90	25.00	22.00	21.20	18.60	19.00	25.90	24.90
202	$\overline{CKBD}$	25.15	20.70	20.85	18.80	18.50	19.80	19.95	18.50	20.20	25.30	22.05	21.25	19.35	19.00	26.40	25.05
231	CKBD	24.35	25.65	24.00	22.00	23.20	23.30	23.85	23.65	21.60	25.90	25.80	26.20	25.70	25.40	24.60	24.60
231	$\overline{CKBD}$	23.95	25.65	24.00	22.10	22.90	23.15	24.70	22.40	22.25	25.90	25.25	26.35	24.70	24.75	24.10	24.15
247	CKBD	23.75	24.80	24.40	23.75	21.40	22.40	23.25	24.25	22.60	20.30	20.20	22.35	22.50	24.00	20.90	22.40
247	$\overline{CKBD}$	23.80	23.70	23.90	23.80	21.75	22.55	22.90	23.40	23.00	20.35	20.95	20.90	22.65	22.80	20.70	22.30
256	CKBD	23.95	22.55	23.25	23.05	20.70	22.15	20.70	21.55	21.80	22.15	25.85	23.85	21.40	20.45	21.70	21.55
256	$\overline{CKBD}$	25.00	23.05	23.40	23.20	21.30	23.05	21.25	20.00	22.50	22.40	24.85	22.75	20.55	20.80	20.65	21.55
259	CKBD	24.80	23.45	21.10	22.70	21.20	20.95	20.65	24.45	22.25	20.80	19.90	20.55	22.45	19.60	20.60	21.65
259	$\overline{CKBD}$	24.30	20.00	22.15	22.05	21.85	20.80	22.85	24.45	20.90	21.25	19.75	21.70	22.05	20.10	21.05	21.50
508	CKBD	21.90	21.55	24.65	20.45	20.25	22.15	21.95	21.20	20.40	23.30	22.45	20.50	21.80	20.65	21.65	20.00
508	$\overline{CKBD}$	22.25	22.25	24.70	20.40	20.65	23.20	21.60	22.45	21.80	23.60	21.60	19.80	20.85	21.10	21.70	23.00
519	CKBD	23.35	26.15	25.75	24.90	25.15	23.40	22.75	23.75	24.10	24.10	26.65	25.75	23.35	23.65	24.70	26.10
519	$\overline{CKBD}$	24.45	26.90	26.35	23.40	24.90	24.60	22.75	26.25	25.70	23.85	26.70	24.95	22.65	23.80	24.85	26.05
522	CKBD	20.75	21.80	21.50	23.00	20.50	21.50	21.55	22.05	20.30	22.75	21.95	20.15	21.00	21.40	20.40	20.75
522	$\overline{CKBD}$	21.15	22.40	20.90	22.80	21.10	21.20	21.35	21.40	20.35	22.55	20.10	19.75	21.00	21.60	20.05	20.05
529	CKBD	19.95	19.15	20.05	22.85	21.15	19.15	20.65	19.65	19.85	20.00	19.85	20.85	20.50	20.90	20.85	21.25
529	$\overline{CKBD}$	20.65	19.80	20.00	21.30	19.90	21.10	23.90	21.15	20.65	21.50	21.60	21.00	20.10	20.95	20.15	18.70

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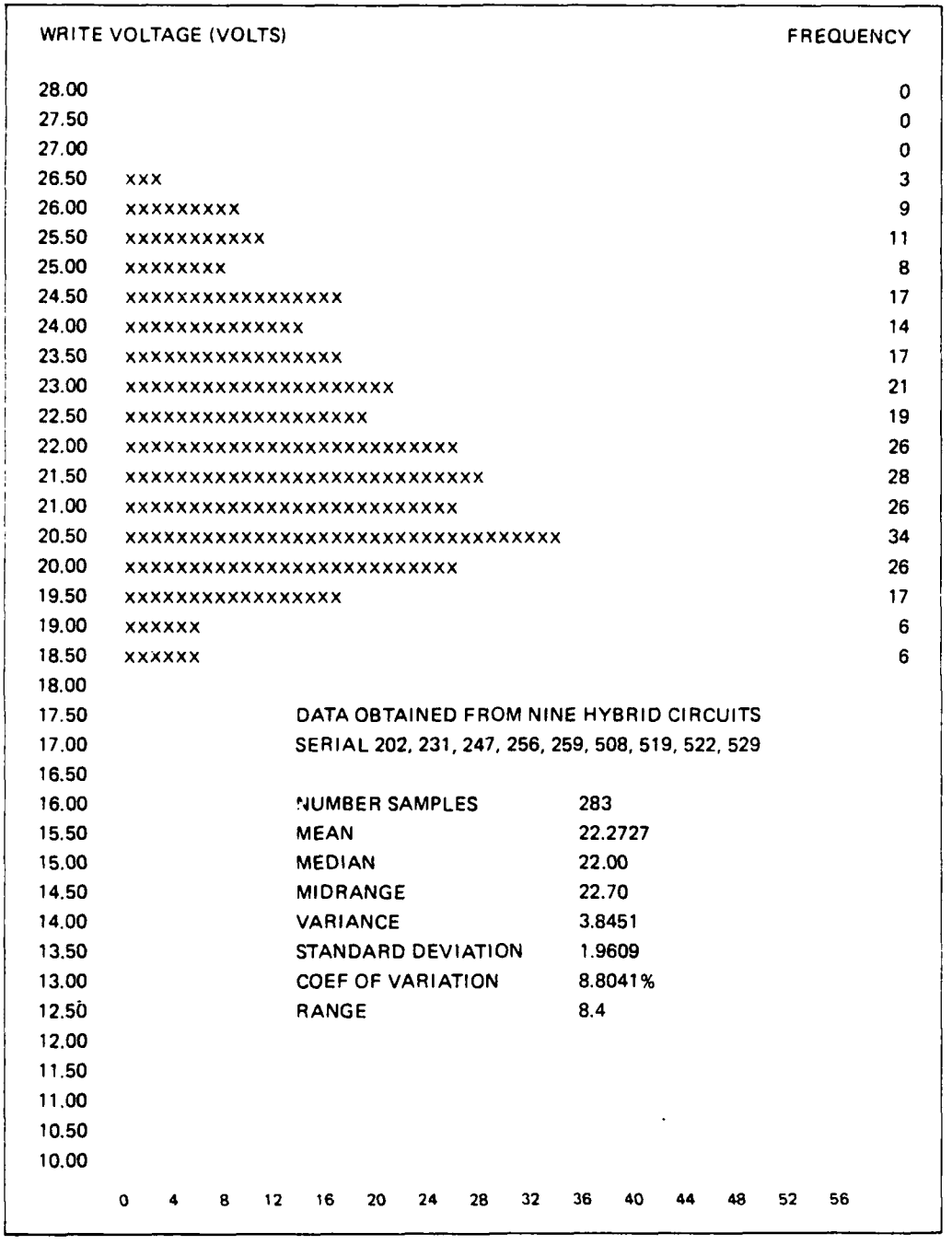

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Figure 1-6. Post Burn-In Minimum Write Voltage Histogram

Table 1-8. Post Burn-In Slope

HYBRID CIRCUIT SERIAL	PATTERN	SLOPE (DECADES PER VOLT)															
		CHIP 1	CHIP 2	CHIP 3	CHIP 4	CHIP 5	CHIP 6	CHIP 7	CHIP 8	CHIP 9	CHIP 10	CHIP 11	CHIP 12	CHIP 13	CHIP 14	CHIP 15	CHIP 16
202	CKBD	7.89	3.21	2.91	2.31	3.49	17.48	3.08	2.43	2.93	5.81	3.59	5.17	3.47	5.78	4.66	4.27
202	$\overline{\text{CKBD}}$	8.09	3.99	2.34	3.05	3.22	2.89	2.86	2.77	2.50	4.14	4.00	7.80	3.47	12.43	2.77	3.88
231	CKBD	4.57	3.44	0.58	3.50	3.54	2.87	3.91	1.96	3.45	11.45	3.89	7.35	4.31	3.00	4.20	3.53
231	$\overline{\text{CKBD}}$	4.32	3.60	5.26	3.46	4.02	2.57	5.34	4.42	3.07	9.52	3.62	7.18	3.74	4.19	5.85	3.99
247	CKBD	3.92	3.26	3.25	4.20	3.24	3.13	4.81	3.62	5.19	4.54	3.46	3.24	6.12	3.95	3.63	4.06
247	$\overline{\text{CKBD}}$	4.34	4.70	3.62	3.79	3.61	3.08	4.30	4.90	4.14	4.20	3.74	4.17	3.92	3.75	3.69	3.77
256	CKBD	6.04	7.43	4.12	3.20	3.09	4.31	2.15	2.63	2.67	2.64	4.32	8.91	2.73	1.93	2.41	3.49
256	$\overline{\text{CKBD}}$	4.73	6.73	4.63	3.62	2.68	5.04	2.28	3.01	3.13	2.28	5.12	6.38	2.28	2.11	2.50	2.88
259	CKBD	5.02	3.55	6.54	2.96	1.95	3.83	3.65	11.07	2.80	3.90	2.85	4.35	2.82	3.32	3.39	3.17
259	$\overline{\text{CKBD}}$	5.02	3.49	5.05	2.82	2.66	3.26	2.96	12.64	3.16	3.88	3.84	4.08	2.91	3.13	3.62	2.95
508	CKBD	4.62	3.36	6.14	2.14	2.32	2.95	3.19	1.80	3.35	3.93	3.15	2.41	2.93	4.72	4.40	2.70
508	$\overline{\text{CKBD}}$	4.64	2.88	5.47	2.53	2.41	2.44	3.19	3.78	2.64	3.62	3.56	1.62	4.39	5.56	3.75	2.00
519	CKBD	3.83	6.14	4.14	3.29	3.80	2.72	3.86	4.12	6.51	3.69	3.51	5.74	4.51	5.54	3.26	9.89
519	$\overline{\text{CKBD}}$	4.13	5.86	2.71	3.07	3.32	2.20	4.60	2.93	3.82	7.44	4.95	4.75	4.71	6.12	2.50	8.44
522	CKBD	2.69	3.85	2.87	2.52	2.80	2.87	2.90	3.10	3.48	3.76	1.68	3.19	2.97	3.75	3.54	2.85
522	$\overline{\text{CKBD}}$	3.00	3.20	3.07	3.17	2.67	3.69	2.95	2.80	3.32	2.99	2.50	2.87	3.14	2.78	3.13	2.85
529	CKBD	4.16	3.92	4.55	4.36	3.58	5.00	4.27	4.01	5.00	5.08	4.41	4.70	5.00	3.33	4.13	3.13
529	$\overline{\text{CKBD}}$	4.36	4.72	4.03	3.86	4.44	3.29	3.28	3.38	3.52	4.03	3.20	3.91	4.63	4.25	4.76	4.48

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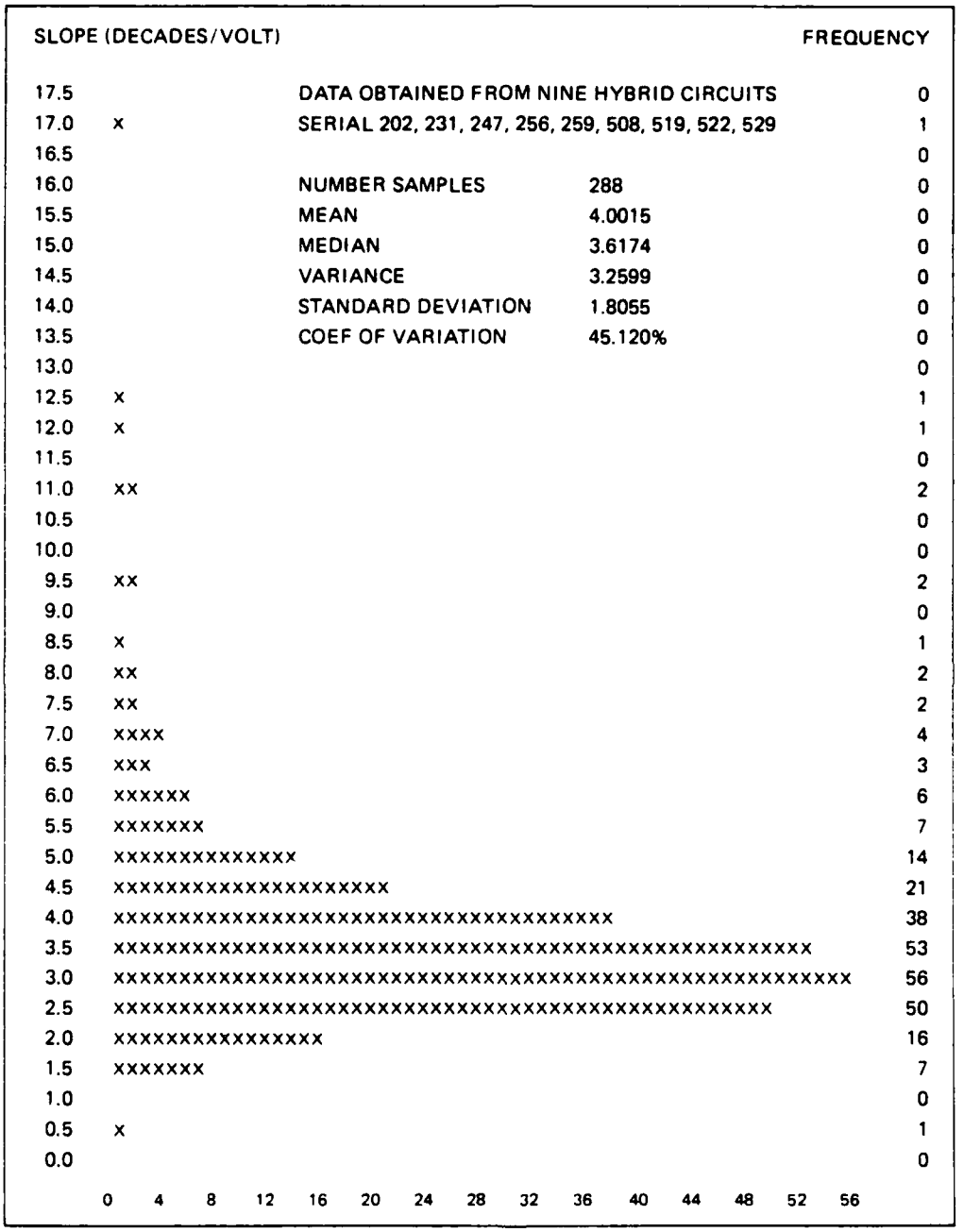

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Figure 1-7. Post Burn-In Slope Histogram

Table 1-9. Temperature Test Data for Eight Samples

DEVICE SERIAL	AMBIENT TEMPERATURE °C	CHECKERBOARD PATTERN				CHECKERBOARD BAR PATTERN			
		MIN V VOLTS	SLOPE DECADES/V	LOG TR LOG HRS	TR HOURS	MIN V VOLTS	SLOPE DECADES/V	LOG TR LOG HRS	TR HOURS
129	-55	24.05	6.9816	37.8052	6.386e37	24.10	5.1326	26.5357	3.433e26
	+25	23.55	7.0754	41.8687	7.391e41	23.25	5.2510	31.6418	4.383e31
	+125	22.30	8.2270	59.5976	3.959e59	23.35	5.1781	35.8042	6.371e35
130	-55	24.00	5.6158	29.8971	7.891e29	24.10	5.1466	26.6177	4.147e26
	+25	23.55	8.1541	48.8358	6.852e48	23.40	6.2485	37.4376	2.739e37
	+125	22.30	6.8249	48.7845	6.089e48	22.35	5.2522	36.3895	2.452e36
132	-55	23.45	3.6667	20.2119	1.629e20	23.50	3.6272	19.8061	6.399e19
	+25	22.45	4.3325	28.9173	8.267e28	22.70	4.1855	26.7845	6.088e26
	+125	21.55	4.2864	32.4093	2.566e32	21.35	3.7971	29.0414	1.100e29
133	-55	24.30	3.2449	14.6940	4.943e14	24.60	2.9917	12.3318	2.147e12
	+25	23.45	3.4829	18.9755	9.451e18	23.80	3.9998	21.0179	1.042e21
	+125	22.30	4.8651	33.6957	4.963e33	22.55	3.9013	25.2463	1.763e25
134	-55	24.60	5.0429	23.4902	3.092e23	24.65	4.4540	20.0611	1.151e20
	+25	24.55	5.7769	27.6869	4.863e27	24.20	4.9691	25.0390	1.094e25
	+125	23.00	6.9403	44.7795	6.018e44	22.85	5.5222	35.6366	4.331e35
136	-55	23.15	3.4273	19.6848	4.840e19	23.10	3.2035	18.2918	1.958e18
	+25	22.60	3.9807	25.6645	4.619e25	22.60	4.0052	25.8335	6.815e25
	+125	21.60	4.4723	33.7665	5.841e33	21.60	5.1127	39.1386	1.376e39
137	-55	24.60	2.8980	11.8556	7.171e11	22.65	4.2161	27.2198	1.659e27
	+25	24.15	3.9499	19.3393	2.184e19	24.65	3.2013	13.3269	2.123e13
	+125	22.90	4.1683	25.8334	6.814e25	21.30	5.2844	42.1726	1.488e42
138	-55	23.35	3.8937	22.1035	1.275e22	24.90	3.7298	15.2103	1.623e15
	+25	22.95	4.3325	26.6974	4.982e26	24.30	4.4320	21.4588	2.876e21
	+125	22.50	5.1132	34.5343	3.422e34	23.40	4.7344	27.4739	2.978e27

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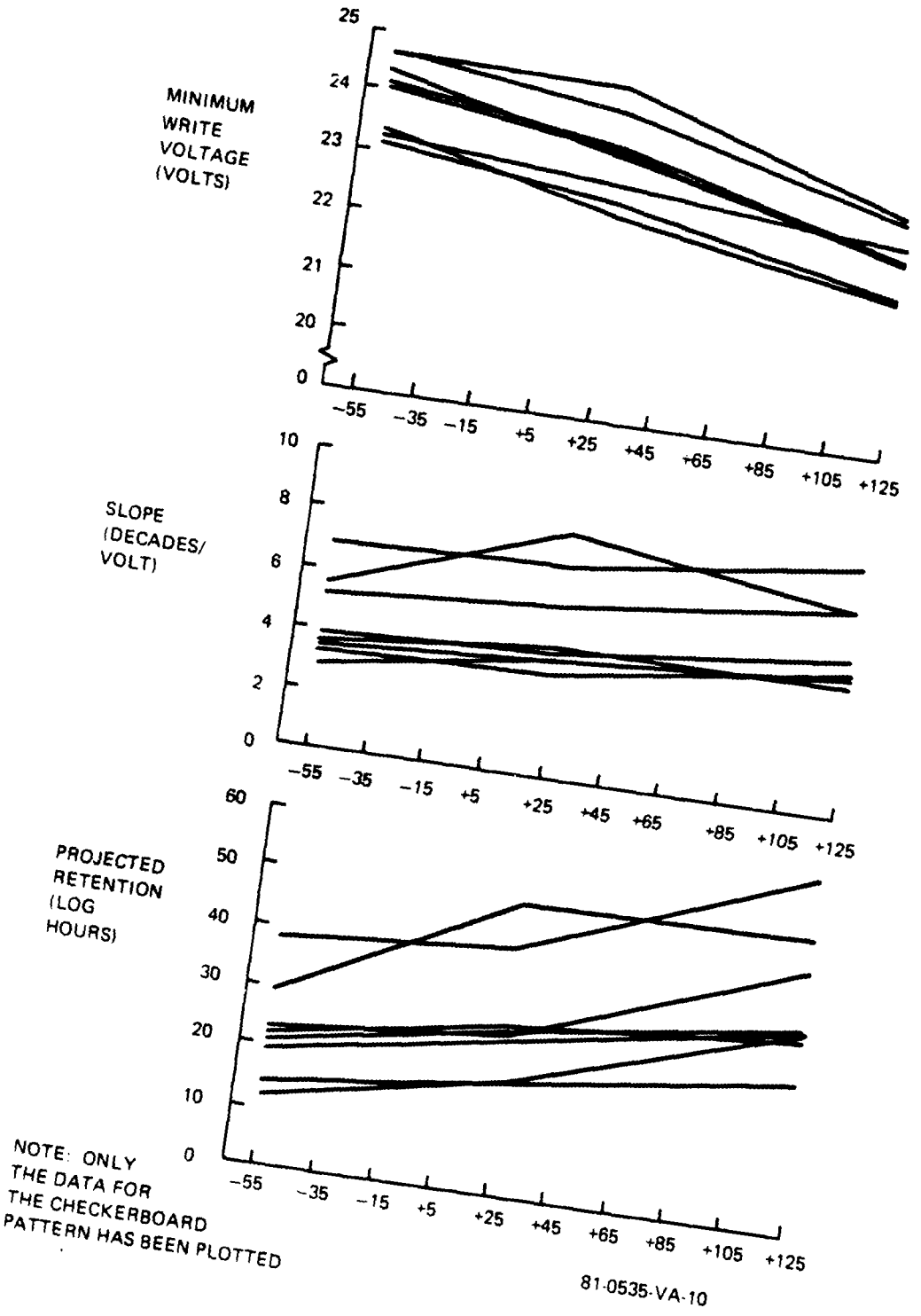


Figure 1-8. Temperature Trend Plots for Eight Samples

1.3.4 Erase-Write Time Effects

An experiment was performed to examine the effect of erase mode, erase time and write time on the RP test parameters minimum write voltage, slope and projected retention. One BORAM 6008 device in a DIP package was subjected to a series of 18 RP tests. The conditions and results for each test are summarized in table 1-10.

In effect, a three-factor experiment was performed where three different response variables existed. The factors and levels were:

Factor	No. Levels
a. Erase Mode	2
b. Erase Time	3
c. Write Time	3

The model for means is:

$$y_{ijkl} = \mu + \alpha_i + \beta_j + \gamma_k + (\alpha\beta)_{ij} + (\alpha\gamma)_{ik} + (\beta\gamma)_{jk} + (\alpha\beta\gamma)_{ijk} + e_{ijkl}$$

$i = 1$ to 2; $j = 1$ to 3; $k = 1$ to 3; $l = 1$ to 2

The issue at hand is whether any of the factors affect RP test results. In other words, test the hypothesis that the mean values associated with each level of a factor are equal.

Table 1-10. RP Test Results for Varied Pulsewidths

ERASE MODE	ERASE TIME μSEC	WRITE TIME μSEC	CHECKERBOARD			CHECKERBOARD BAR		
			minV VOLTS	SLOPE DEC/V	RETENTION HOURS	minV VOLTS	SLOPE DEC/V	RETENTION HOURS
CHIP	1000	200	21.40	2.3913	5.682e16	20.60	3.0345	5.550e24
		100	22.40	2.6184	1.251e16	21.55	2.6579	4.247e18
		20	25.35	2.2686	5.177e06	24.50	2.7225	1.335e11
	400	200	21.45	2.3732	3.146e16	20.60	2.4950	4.348e19
		100	22.45	2.6719	2.357e16	21.60	2.8414	1.152e20
		20	25.35	2.1860	2.054e06	24.55	2.9066	1.044e12
	200	200	21.45	2.1726	5.865e14	20.65	2.8196	3.780e22
		100	22.45	2.5290	1.967e15	21.60	2.7061	8.435e18
		20	25.40	2.4759	3.660e07	24.55	2.7993	2.637e11
WORD	1000	200	21.40	2.2982	8.926e15	20.60	2.8519	1.040e23
		100	22.40	2.5652	4.961e15	21.55	2.5634	6.716e17
		20	25.35	2.4367	3.201e07	24.50	2.7225	1.344e11
	400	200	21.45	2.4293	9.429e16	20.60	2.4945	4.301e19
		100	22.40	2.3418	9.401e13	21.60	2.8909	3.015e20
		20	25.35	2.2252	3.334e06	24.50	2.6524	5.673e10
	200	200	21.45	2.4374	1.079e17	20.60	2.5507	1.443e20
		100	22.45	2.8056	2.405e17	21.60	3.0480	6.227e21
		20	25.35	2.2905	6.657e06	24.50	2.7990	3.628e11

81-0535-TA-18

Analysis of variance computations were carried out for each of the response variables, and are presented in tables 1-11 to 1-13. The computed F numbers show that erase mode and erase time do not significantly modify RP test results. Write time did not significantly affect slope. Write time was shown to significantly affect the minimum write voltage and the log time projection.

Given that write voltage and the log of projected retention are functions of write time, the data for each data pattern was subjected to regression analysis.

Pattern	Equation	Correlation Coef
CKBD	$V = 30.491 - 3.972\ \log tp$	0.9985
$\overline{CKBD}$	$V = 29.629 - 3.985\ \log tp$	0.9985
CKBD	$\log t_r = -5.669 + 10.0047\ \log tp$	0.9532
$\overline{CKBD}$	$\log t_r = -2.208 + 10.5684\ \log tp$	0.9496

These findings seem to be consistent with current understanding as to how the RP test works. The use of nominal voltage during erase forces the DSP memory transistors into what is essentially the fixed threshold state. Thus, erase mode and erase time should not strongly affect RP test response variables.

Table 1-11. ANOVA for Erase and Write Time Effects on Minimum Voltage

SOURCE OF VARIATION	SUM OF SQUARES	DEGREES OF FREEDOM	MEAN SQUARE	F
MAIN EFFECT				
ERASE MODE	0.002	1	0.002	0.005
ERASE TIME	0.009	2	0.004	0.013
WRITE TIME	99.647	2	49.823	142.437
TWO FACTOR INTERACTION				
ERASE MODE × ERASE TIME	0.001	2	0.000	0.001
ERASE MODE × WRITE TIME	0.001	2	0.000	0.001
ERASE TIME × WRITE TIME	0.001	4	0.000	0.001
THREE FACTOR INTERACTION				
ERASE MODE × ERASE TIME × WRITE TIME	0.001	4	0.000	0.001
ERROR	6.296	18	0.350	–
TOTAL	105.957	35	–	–

$F_{0.01}\ (2, 18) = 6.01$, $F_{0.05}\ (2, 18) = 3.55$

81-0535 TA 19

Table 1-12. ANOVA for Erase and Write Time Effects on Slope

SOURCE OF VARIATION	SUM OF SQUARES	DEGREES OF FREEDOM	MEAN SQUARE	F
MAIN EFFECT				
ERASE MODE	0.0020	1	0.0020	0.0241
ERASE TIME	0.0371	2	0.0186	0.2268
WRITE TIME	0.1854	2	0.0927	1.1330
TWO FACTOR INTERACTION				
ERASE MODE × ERASE TIME	0.0349	2	0.0175	0.2133
ERASE MODE × WRITE TIME	0.0097	2	0.0049	0.0595
ERASE TIME × WRITE TIME	0.1246	4	0.0311	0.3806
THREE FACTOR INTERACTION				
ERASE MODE × ERASE TIME × WRITE TIME	0.1212	4	0.0303	0.3703
ERROR	1.4727	18	0.0818	–
TOTAL	1.9876	35	–	–

$F_{0.01}$ (2, 18) = 6.01, $F_{0.05}$ (2, 18) = 3.55

81-0535-TA-20

Table 1-13. ANOVA for Erase and Write Time Effects on Log (Time) Projection

SOURCE OF VARIATION	SUM OF SQUARES	DEGREES OF FREEDOM	MEAN SQUARE	F
MAIN EFFECT				
ERASE MODE	0.047	1	0.047	0.004
ERASE TIME	2.004	2	1.002	0.086
WRITE TIME	690.336	2	345.168	29.489
TWO FACTOR INTERACTION				
ERASE MODE × ERASE TIME	2.691	2	1.346	0.115
ERASE MODE × WRITE TIME	0.684	2	0.342	0.029
ERASE TIME × WRITE TIME	9.862	4	2.465	0.211
THREE FACTOR INTERACTION				
ERASE MODE × ERASE TIME × WRITE TIME	6.249	4	1.562	0.133
ERROR	210.690	18	11.705	–
TOTAL	922.564	35	–	–

$F_{0.01}$ (2, 18) = 6.01, $F_{0.05}$ (2, 18) = 3.55

81-0535-TA-21

1.3.5 Endurance Effects

A preliminary investigation as to how the RP test reflects device changes associated with endurance has been initiated. Four unscreened BORAM 6008 chips were cycled in the unbalanced mode with the checkerboard bar pattern using chip erase. The erase time was 1000 microseconds, and the write time was 200 microseconds. A normal 30-volt supply level was applied.

The checkerboard bar pattern used for cycle stress caused one transistor in each two-transistor cell to be erase-write cycled. The other transistor in each cell was subjected to repeated erase pulses. The cycled transistors would be expected to show changes as the cycle stress accumulates. The transistors which are erased over and over would be enjoying a relatively low stress environment, and would not be expected to change characteristics.

It is of interest to see whether the RP test results reflect these expectations. The checkerboard bar RP test should be primarily a function of the stressed transistors. The checkerboard RP test should reflect the unstressed transistors.

In table 1-14, the minimum write voltage shows changes of 1 to 3 volts from initial to 1e7 cycles for the checkerboard bar pattern. Changes from *0.25 to 0.60 volts were observed for the checkerboard* pattern. The data above 1e6 cycles was plotted in figure 1-9. The unstressed side of the devices changed very slightly. The stress side shows a linear shift toward lower voltages. Curve fits of the form Voltage = Slope × Log (Cycles) for the stressed side data yields correlation coefficients of 0.9972 to 0.9999.

Table 1-14. Minimum Write Voltage vs Erase-Write Cycles

ERASE WRITE CYCLES	MINIMUM WRITE VOLTAGE (VOLTS)							
	CHECKERBOARD PATTERN				CHECKERBOARD BAR PATTERN			
	SERIAL 101	SERIAL 102	SERIAL 103	SERIAL 104	SERIAL 101	SERIAL 102	SERIAL 103	SERIAL 104
INITIAL	22.10	21.85	22.55	24.60	23.85	21.00	22.85	22.00
1e6	22.35	21.95	22.80	24.30	23.35	20.65	22.65	20.70
3e6	22.50	22.00	22.80	24.10	22.65	19.95	22.25	19.70
1e7	22.65	22.10	22.90	24.00	21.65	19.30	21.80	18.80
MAX	22.65	22.10	22.90	24.60	23.85	21.00	22.85	22.00
MIN	22.10	21.85	22.55	24.00	21.65	19.30	21.80	18.80
DELTA	0.55	0.25	0.35	0.60	2.20	1.70	1.05	3.20

81-0535-TA-22

Table 1-15 shows the computed slopes. The data above 1e6 cycles is plotted in figure 1-10. Trends are not as clear cut as for the voltage data. The expectation was that transistor changes would become noticeable at 1e7. The RP test showed two of four samples with a marked increase in slope at this stress level .

Figure 1-11 presents the retention projection data for stressed and unstressed memory cells. The results were highly variable with unstressed cells shifting for the most part toward lower retention, and stressed cells toward higher retention.

Table 1-15. Slope vs Erase-Write Cycles

ERASE WRITE CYCLES	MINIMUM WRITE VOLTAGE (VOLTS)							
	CHECKERBOARD PATTERN				CHECKERBOARD BAR PATTERN			
	SERIAL 101	SERIAL 102	SERIAL 103	SERIAL 104	SERIAL 101	SERIAL 102	SERIAL 103	SERIAL 104
INITIAL	6.4259	3.9931	3.7897	2.2980	3.4366	3.8420	4.7723	9.3165
1e6	3.7805	3.7058	3.4876	2.5823	1.8718	2.6101	2.8958	3.2116
3e6	3.8019	3.6773	3.2535	2.6118	1.9234	2.9916	2.5509	3.3209
1e7	3.0549	3.3547	2.7443	2.2738	2.2097	4.1769	2.5512	4.6639
MAX	6.4259	3.9931	3.7897	2.6118	3.4366	4.1769	4.7723	9.3165
MIN	3.0549	3.3547	2.7443	2.2738	1.8718	1.6101	2.5509	3.2116
DELTA	3.3710	0.6384	1.0454	0.3380	1.5648	1.5668	2.2214	6.1049

81-0535-TA-24

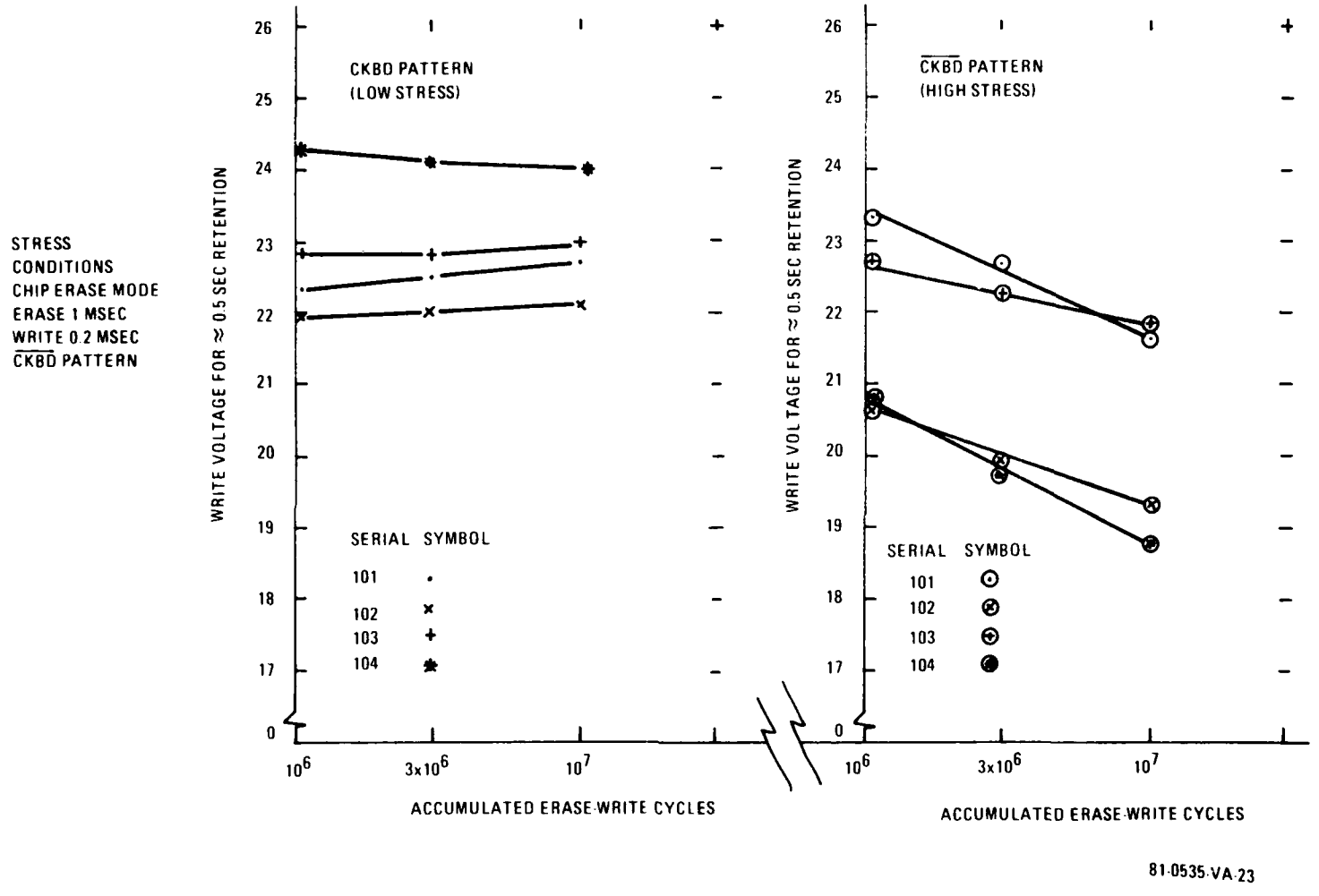


Figure 1-9. Erase-Write Cycles vs Minimum Write Voltage (Unbalanced Stress)

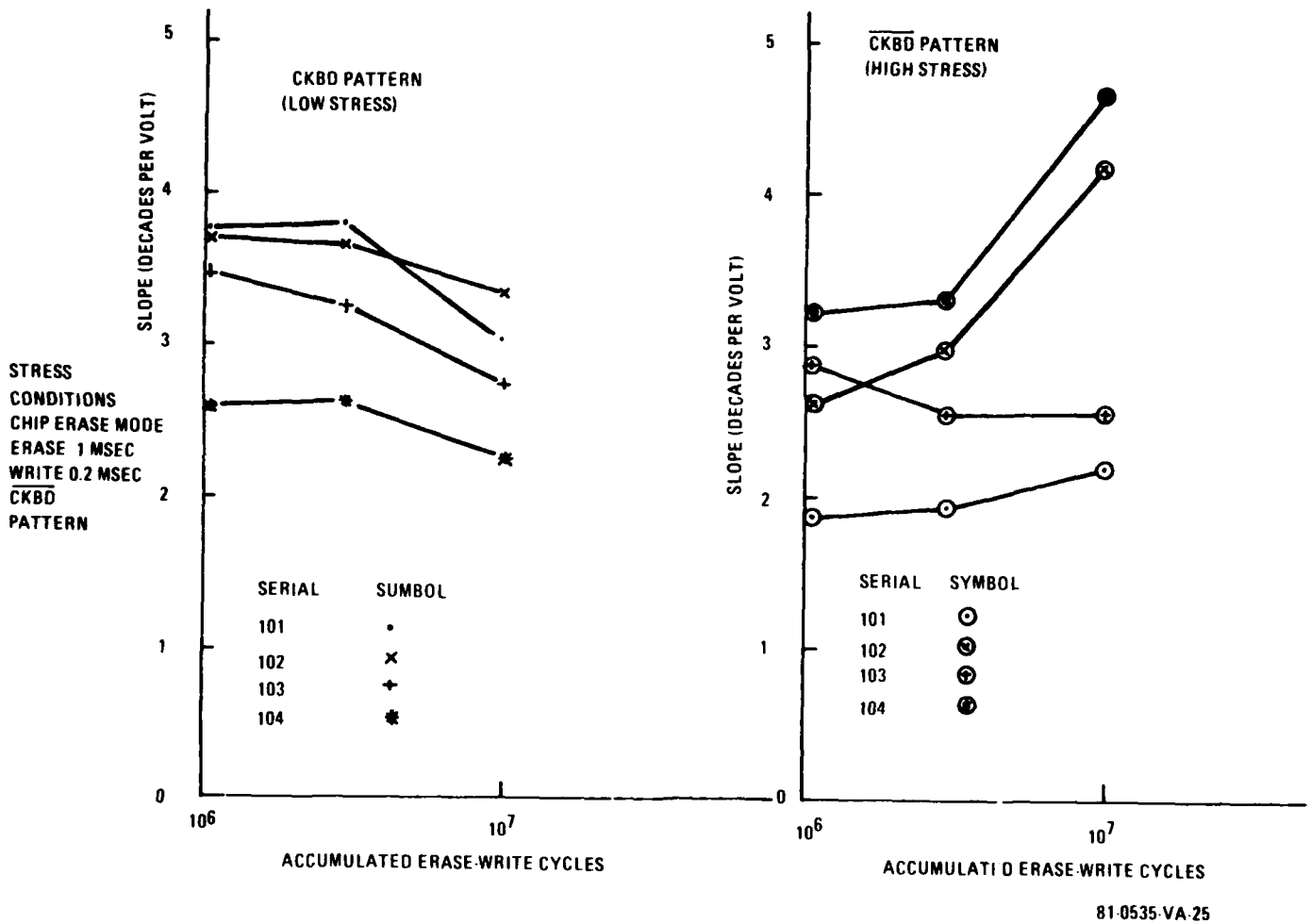


Figure 1-10. Erase-Write Cycles vs Slope (Unbalanced Stress)

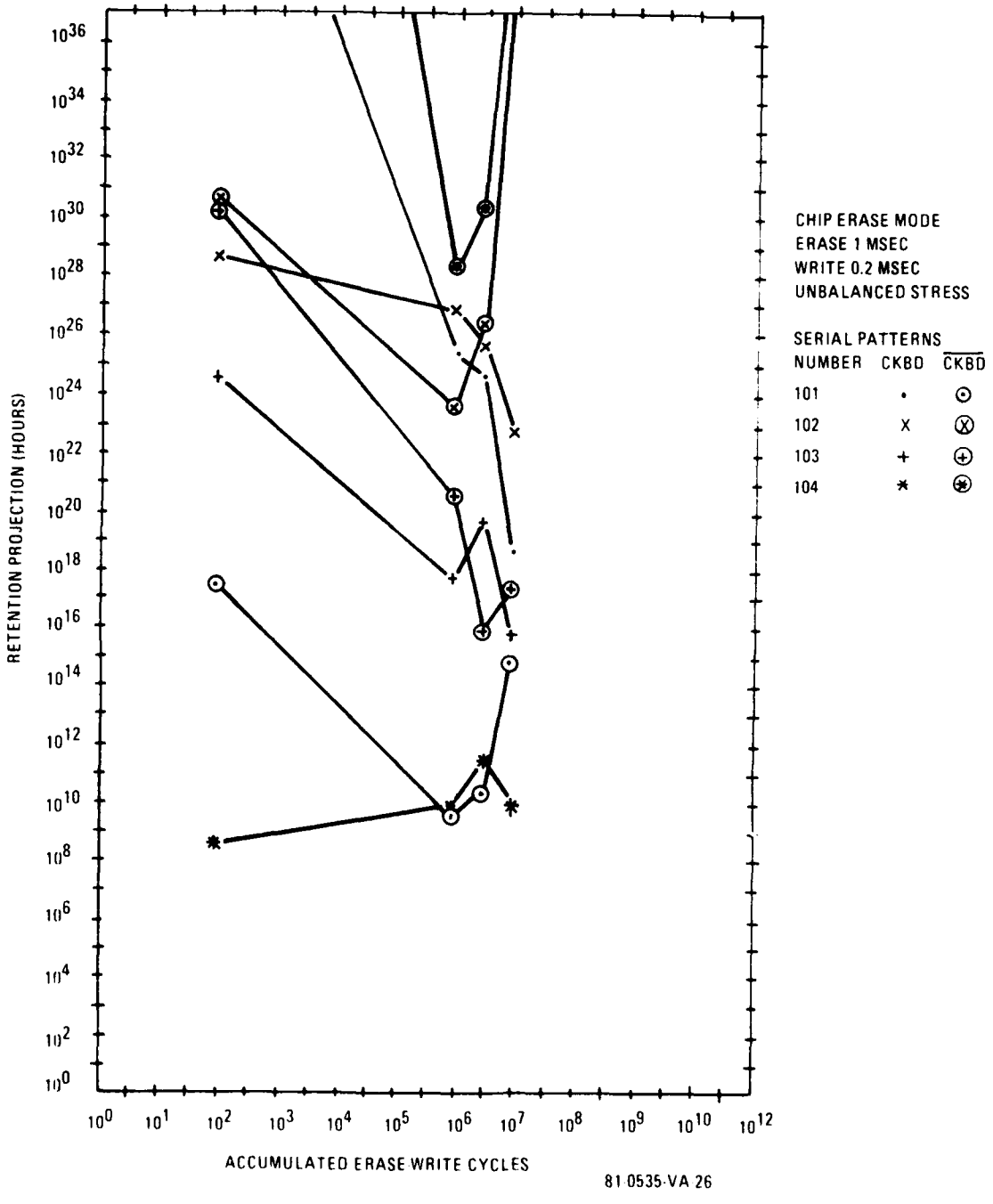


Figure 1-11. Retention Projection vs Erase-Write Cycles

2. CONCLUSIONS

At the current stage of development, the RP test shows some promise of being useful as the basis for a screen to remove defective or suspect devices from the population. Some form of an RP test is visualized as being a part of a comprehensive set of stresses and tests oriented toward endurance-retention characteristics.

The RP test cannot be assumed to provide an accurate estimate of real-time retention. It does, however, appear to provide information directly related to endurance-retention properties of devices. Further work is required to quantitatively define such relationships.

3. PROGRAM FOR NEXT INTERVAL

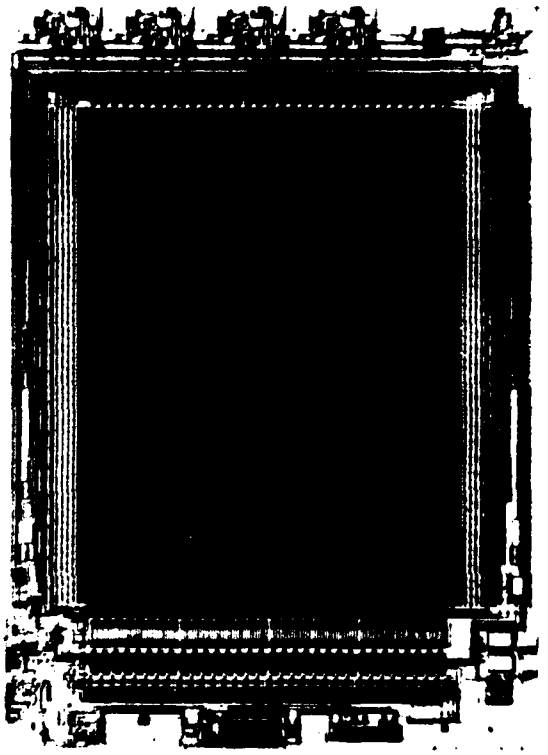
The primary tasks during the next period are the performance of the pilot run, the demonstration of throughput capability, and the continued investigation of the utility of the RP test.

4. PUBLICATIONS AND REPORTS

During the reporting period there were no publications derived directly from this contract effort.

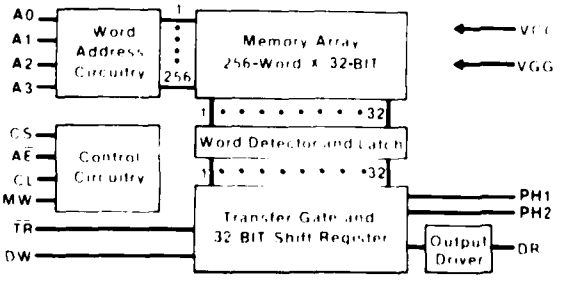
BORAM 6008 Nonvolatile Integrated Circuit Block-Oriented Random-Access Memory Chip

- **8,192-bit block-oriented RAM**
- **Two DSP transistors per cell**
- **Fast Read and Write**
- **128-bit or 8,192-bit erase**
- **High endurance/retention characteristics**
- **< 400 milliwatts power dissipation per chip**



The 6008 chip is an 8,192-bit memory intended for use in block-oriented random-access memory systems. It is normally packaged in multichip hybrid form to achieve high density, but can also be packaged in leadless carriers, flat packages or dual-in-line packages. Use of the MNOS (metal-nitride-oxide semiconductor) technology allows nonvolatile information storage and low power operation. The circuit design uses p-channel metal gate transistors on bulk silicon. Reliable drain source protected (DSP) memory transistors form the memory array. The die measures 139 by 192 mils, and features a 1.26 mil² two-transistor cell. A glass overcoat guards against scratches due to handling. All inputs have protective voltage limiting devices to avoid damage by static charge.

- **15-volt CMOS compatible**
- **Fully decoded and buffered**
- **Tristate output**
- **Military temperature range**
- **Low pin count -- only 15 pads**
- **Static charge protected**



The 6008 contains a fully decoded 256-word by 32-bit RAM and a 32-bit dynamic two-phase shift register. All I/O is accomplished serially through the shift register. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32-bit latch. The RAM and shift register can operate independently. Data stored in the latch may be written into the RAM while new data is shifted into the register.

The address input signals are multiplexed to reduce the pin count. Four bits of the eight-bit address are placed on the address inputs and are latched internal to the chip. Then the last four bits are placed on the address lines and are held steady.

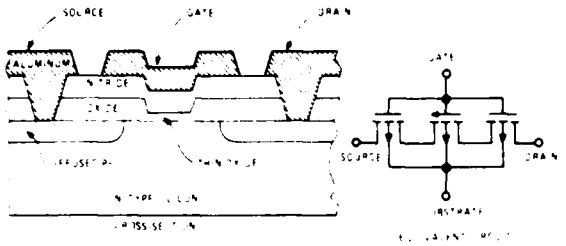
BORAM 6008 Nonvolatile Integrated Circuit Block-Oriented Random-Access Memory Chip

Transistor and Cell Operation

MNOS Device Structure

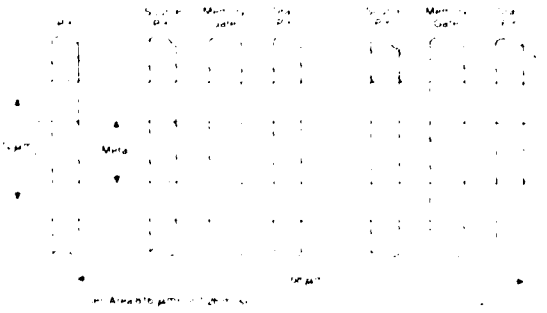
The 6008 device is manufactured using conventional silicon integrated circuit processing. Basic element in the circuit is the metal-nitride-oxide semiconductor (MNOS) transistor. The use of a dual-dielectric insulator composed of silicon nitride and silicon oxide enhances reliability and makes possible the nonvolatile storage of data.

When the oxide layer is made very thin (~20A), electrical signals may be used to insert or remove charge from traps in the nitride close to the nitride-oxide interface. Changes in the insulator charge cause the threshold voltage of the transistor to shift in value. When power is removed the charge in the insulator will be retained for long periods of time. If the oxide layer is made thick (~800A), charge cannot be moved in the insulator, and a nonmemory device results.



DSP Memory Transistor

A reliable memory transistor structure has been achieved by using thick oxide close to the source and drain diffusions to protect the thin memory oxide from electrical fields and/or material imperfections in that region. The so-called "drain-source protected" transistor can be visualized schematically as a memory transistor in series with two nonmemory transistors. An arrow is shown on the gate of a memory transistor symbol to indicate the variable nature of the transistor threshold voltage.



Two-Transistor Storage Cell

Two memory transistors arranged in a balanced differential configuration are used to store one data bit. Storage is a two-step process. First, both transistors in the cell are pulsed into the erased state. Then as a function of the data one or the other of the two transistors is pulsed into the written state. On read out, the sense circuit effectively compares the threshold voltages of the two transistors to determine whether a logic one or logic zero was stored. The difference between the threshold voltages is called the logic window voltage.

Erase-Write Operation

Application of a positive gate to source and substrate potential will cause a positive shift in the threshold voltage of a memory transistor. This most positive threshold level is called the "erased" state. Similarly, application of a negative gate voltage will shift the threshold negative into the "written" state.

Repeated erase-write cycles cause changes in the characteristics of the memory transistor. The magnitude and importance of these changes is a function of the applied voltage levels, waveshapes, and duration. For a given set of operating conditions, the net effect of transistor changes is an alteration of the expected nonvolatile retention time.

BORAM 6008 Nonvolatile Integrated Circuit Block-Oriented Random-Access Memory Chip

Absolute Maximum Chip Ratings

Temperature Range

Operating	**−55°C to +125°C**
Storage	**−65°C to +150°C**

Voltage Range
Voltages Referenced to VCC

$\overline{CS}$	+0.5V to −37V
VGG	+0.5V to −32V
Other Inputs	+0.5V to −20V

Endurance and Retention

As the transistors in a memory cell accumulate erase-write cycles, the number of hours the cell can be expected to retain data is reduced. A rule of thumb observation for cells stressed using standard operating conditions is that

$$\text{retention} > \frac{10^{12} \text{ hours}}{\text{accumulated erase-write cycles}}$$

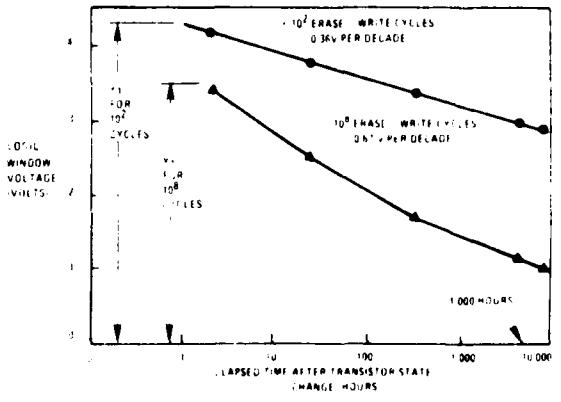
Prospective users should do an analysis of the expected number of erase-write cycles over the life time of the memory system. System specifications should be selected to be well within the rule of thumb guideline, and should also consider the practical aspects of verifying a specific retention requirement.

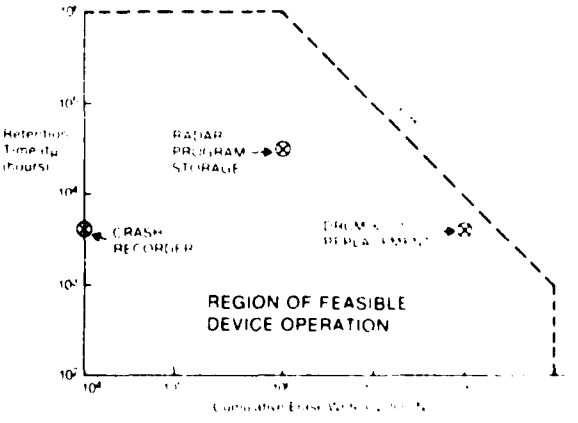
Standard Operating Conditions

VCC	+15V
VGG	−15V
$\overline{CS}$	+15V to −20V
Erase Time	1000 μsec
Write Time	200 μsec

1 YEAR 8 766 HOURS
3 YEAR 26 298 HOURS
5 YEAR 43 830 HOURS

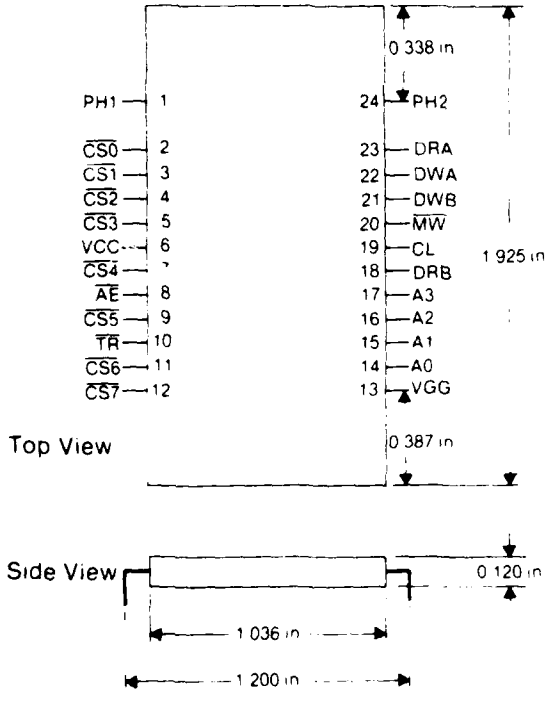
ERASE −25 VOLTS 1 msec
WRITE −25 VOLTS 0.2 msec





BORAM 6008 Nonvolatile Integrated Circuit
Block-Oriented Random-Access Memory Chip

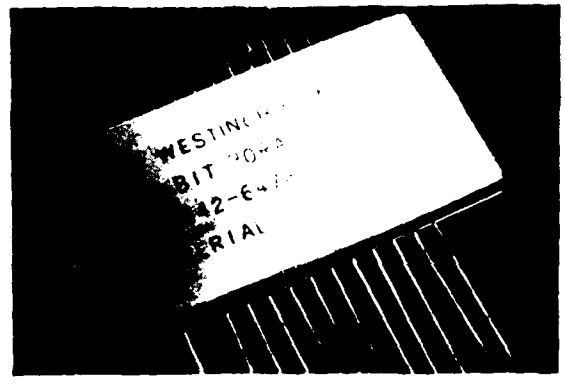
BORAM Multichip Hybrid Microcircuit
Westinghouse Part 647R527G02



Weight 16.5 grams
Thermal Resistance θ_{JC} 5°C Watt

Hybrid Circuit Capacitance

Clock Inputs	PH1, PH2	135 pf
Chip Select Inputs	$\overline{CS0}$ to $\overline{CS7}$	35 pf
Control Inputs	$\overline{AE}$, $\overline{MW}$, $\overline{TR}$	80 pf
Clear Input	CL	160 pf
Address Inputs	A0 to A3	90 pf
Write Data Inputs	DWA, DWB	40 pf
Read Data Outputs	DRA, DRB	60 pf

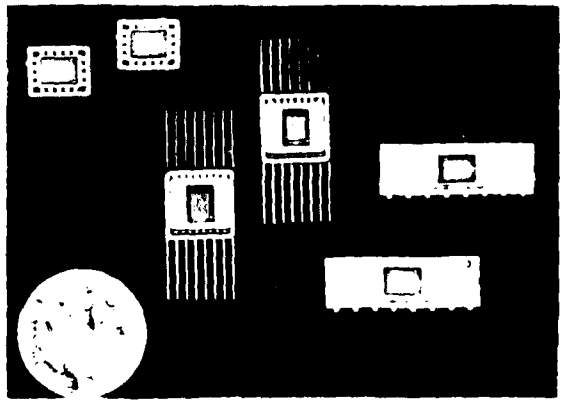


Memory Card Layout Data

Leads: 0.015-in. wide, 0.010-in. thick, 0.100-in. centers
Pin 1 to 2 and 23 to 24 spaced 0.200 inches
Package height: 0.125 in. maximum
On 0.100-in. grid the package footprint is 1.3 x 2.0 in.

Alternative Packages

This data sheet is restricted to a description of the 6008 device mounted in a multichip hybrid circuit. The device can be mounted in other types of package. Dual-in-line, flat package and leadless carrier configurations have been used.



BORAM 6008 Nonvolatile Integrated Circuit
Block-Oriented Random-Access Memory Chip

Circuit Operating Concepts

To store data two operations must be performed. First, the memory cells must be erased or cleared using the clear (CL) signal. Second, the data must be written into the cell using the memory write ($\overline{MW}$) signal. The 6008 design allows erasure of the entire 8,192 cells with one pulse, or optionally allows erasure of 128 cells as a function of address inputs and control signal sequence. Writing takes place in 32-bit words as a function of address inputs and control signal sequence.

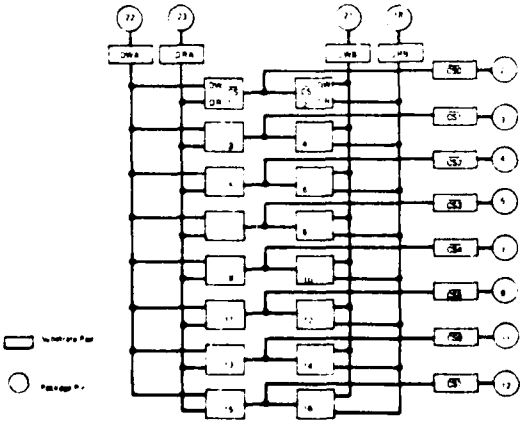
Sixteen BORAM 6008 devices are packaged in one hybrid microcircuit. Half of the 24 pins of the hybrid are bused to all chips. This includes the power supply inputs, control signals and address inputs. Chips are enabled in pairs, and eight chip select signals are provided. Only one of the chip select signals is allowed to be active at any given time.

The data lines for the odd numbered chips in a hybrid are bused. Similarly, the even numbered chip data lines are on a separate bus. These two data buses (DRA and DRB) are tristate. When all chip select lines ($\overline{CS0}$ to $\overline{CS7}$) are high, all eight shift register outputs (DR) on each bus are in the high impedance state. When one chip select line is low, one chip on each bus becomes active and drives the bus.

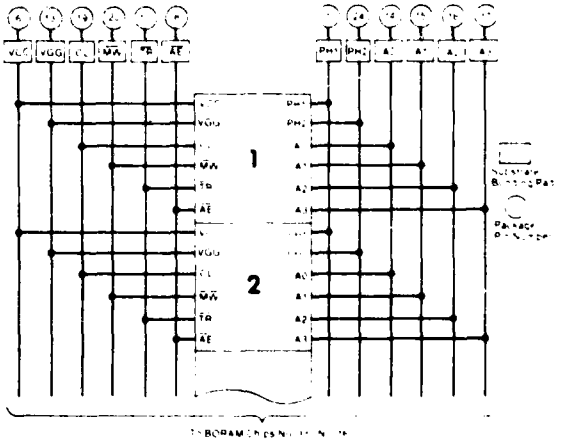
Each BORAM 6008 chip consists of a 256-word by 32-bit RAM and a 32-bit shift register. All input signals except chip select ($\overline{CS}$) swing from +15 volts to ground. The high level chip select signal swings from +15 to −20 volts. Address inputs to the RAM are multiplexed and latched internally to reduce the device pin count. The data output line (DR) is tristate, and will enter the high impedance state if $\overline{CS}$ is high.

A first principle of BORAM system design is to exploit the memory nonvolatility. Individual chips should be power switched by controlling VGG. Devices should be powered up only for the duration of a data transaction. At the beginning of an operation, the VGG level is applied and then the $\overline{CS}$ is applied. The chip select signal acts as an "on chip" power switch, and enables the functional elements of the device.

To read out data, the addresses are set up and the access enable ($\overline{AE}$) signal is used to enable and initiate the data sense process. When the data is stable in the 32-bit latch, it is moved in parallel to the shift register using the transfer ($\overline{TR}$) signal. Data is then taken out of the data read (DR) terminal using the two-phase clocks PH1 and PH2 to empty the register.



I/O and Chip Select Connections



Bused Connection

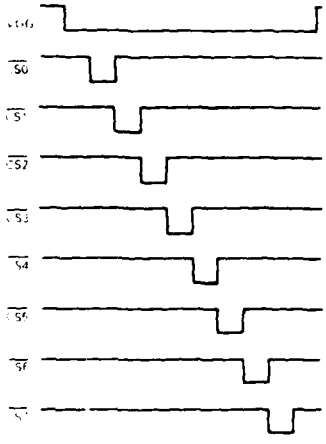
BORAM 6008 Nonvolatile Integrated Circuit Block-Oriented Random-Access Memory Chip

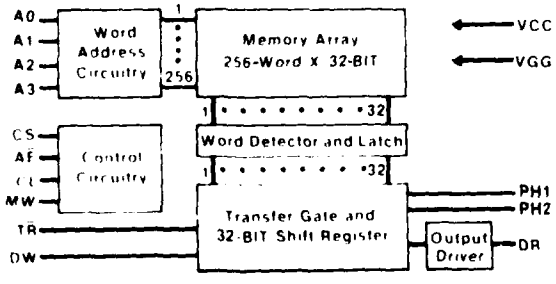
Hybrid Circuit Operation

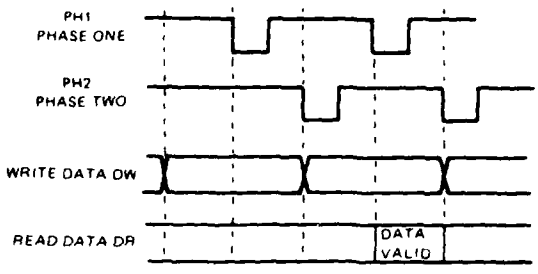
Normally some type of microprogrammed controller will be used to operate the BORAM hybrid circuit. Typical waveform sequences for accomplishing read and write are shown below. A logic flow chart keyed to the waveforms illustrates the software or firmware subroutine structure. The examples treat the case of reading or writing sequentially through the entire address range of the hybrid circuit.

To start operation without disturbing the contents of the memory chips the clear (CL) signal must be held at ground before any chip select (CS) is enabled. During device operation only one CS signal should be selected at any given time. The sequence for one pass through the hybrid is shown in the figure.

Chip Select Sequence







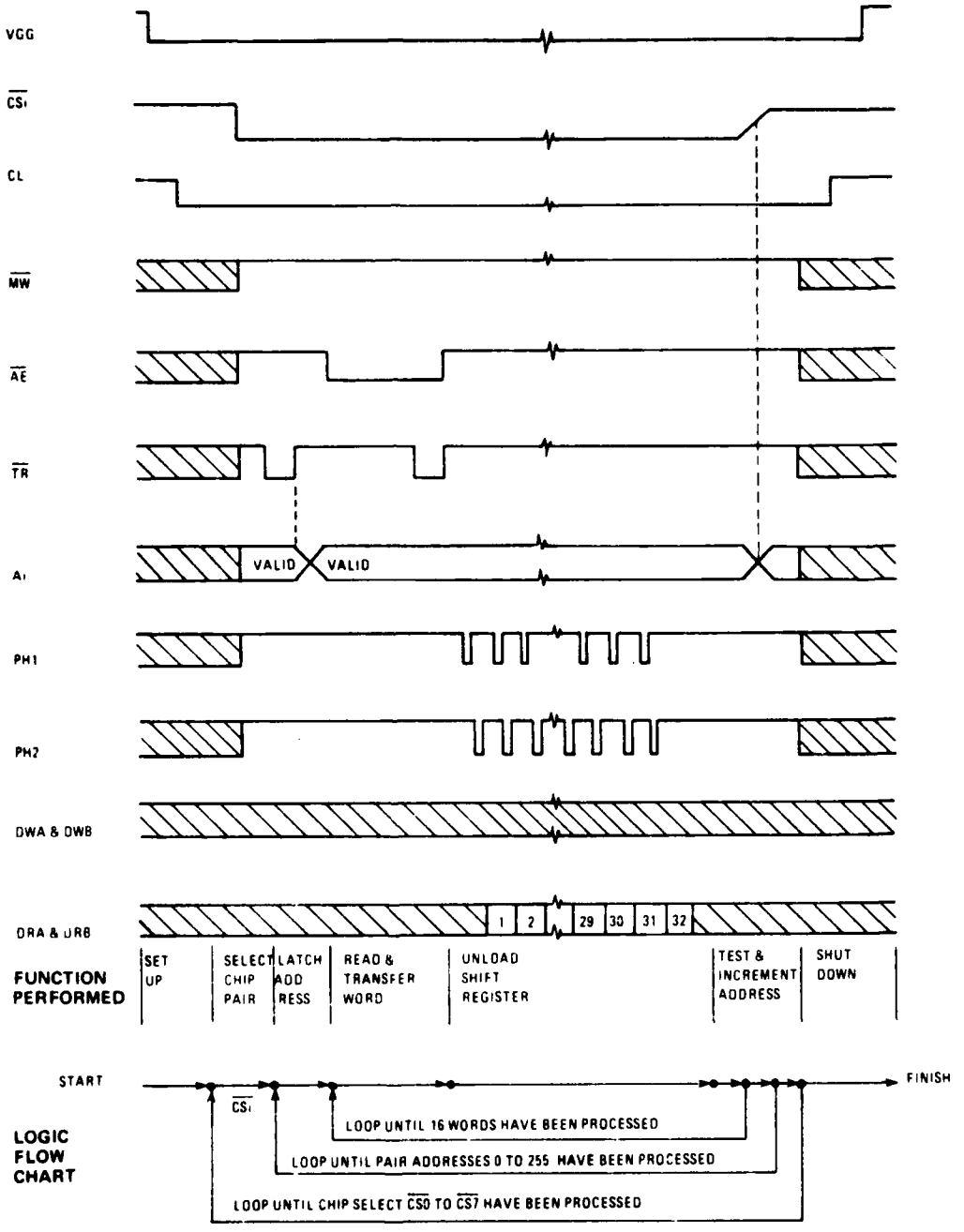
Simplified Clock and Data Timing

The individual functions required to operate the BORAM hybrid are quite simple, and do not involve any critical timing. The block diagram should be used to help visualize the events. Operation of the shift register is accomplished using conventional nonoverlapping two-phase clocking. The register will operate from 1 kHz to 1 MHz. Clock pulsewidths of 250 nanoseconds work well over the temperature range. Input data must become valid before and during PH1. Output data will become valid within 250 nanoseconds of the leading edge of PH2. A simplified trouble-free approach to timing is to setup write data on the leading edge of PH2, and to sample read data on the leading edge of PH1.

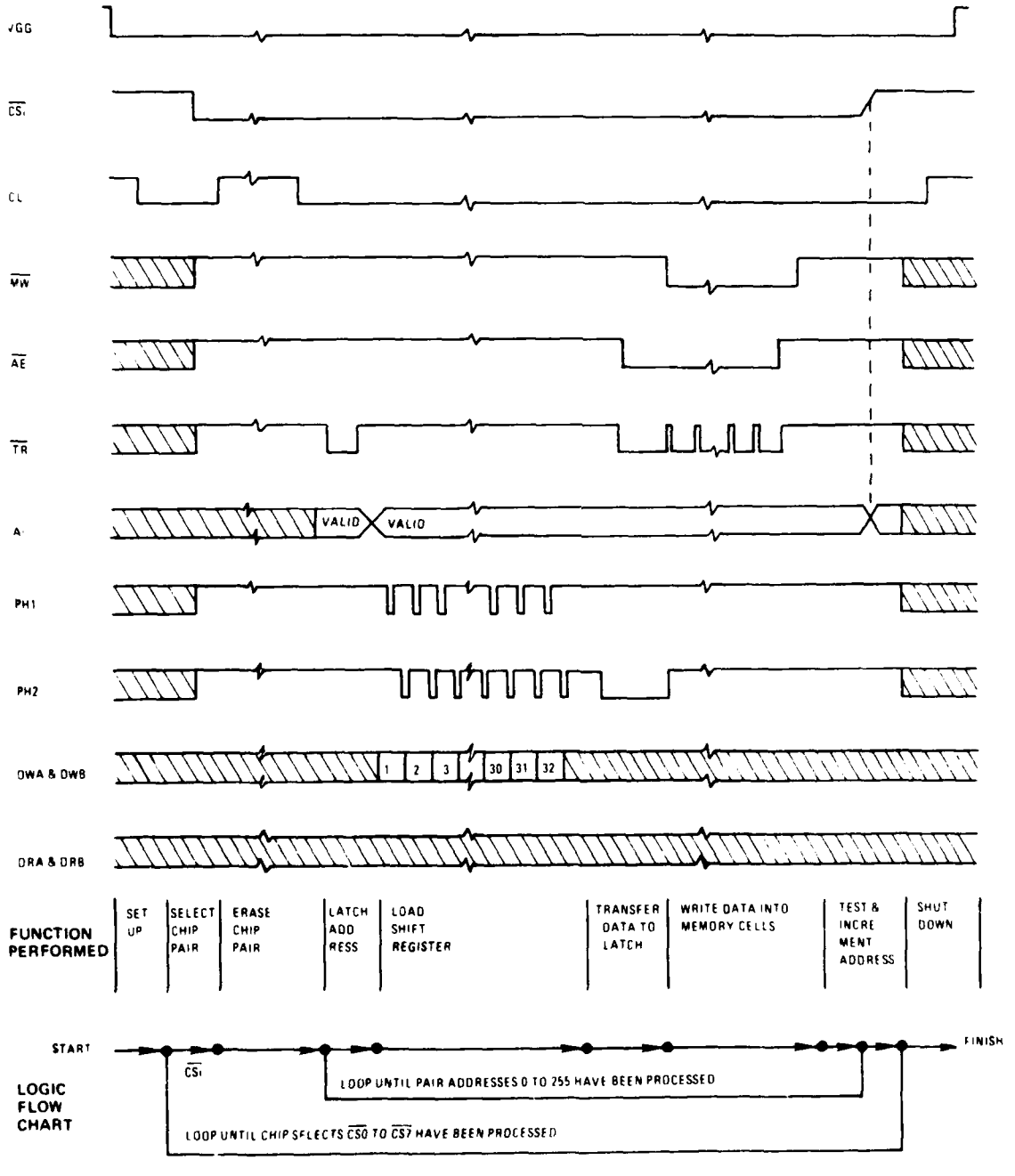
Signal Amplitude Requirements

Signal Symbol	Worst Waveform Levels (V_{CC} = +15V, V_{GG} = −15V)	
	High Level Volts	Low Level Volts
$\overline{AE}$, $\overline{TR}$, $\overline{MW}$, DWA, DWB, A0, A1, A2, A3	≥ 14.00	≤ 3.00
PH1, PH2, CL	≥ 14.00	≤ 0.75
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$, $\overline{CS5}$, $\overline{CS6}$, $\overline{CS7}$	≥ 14.00	≤ −19.65

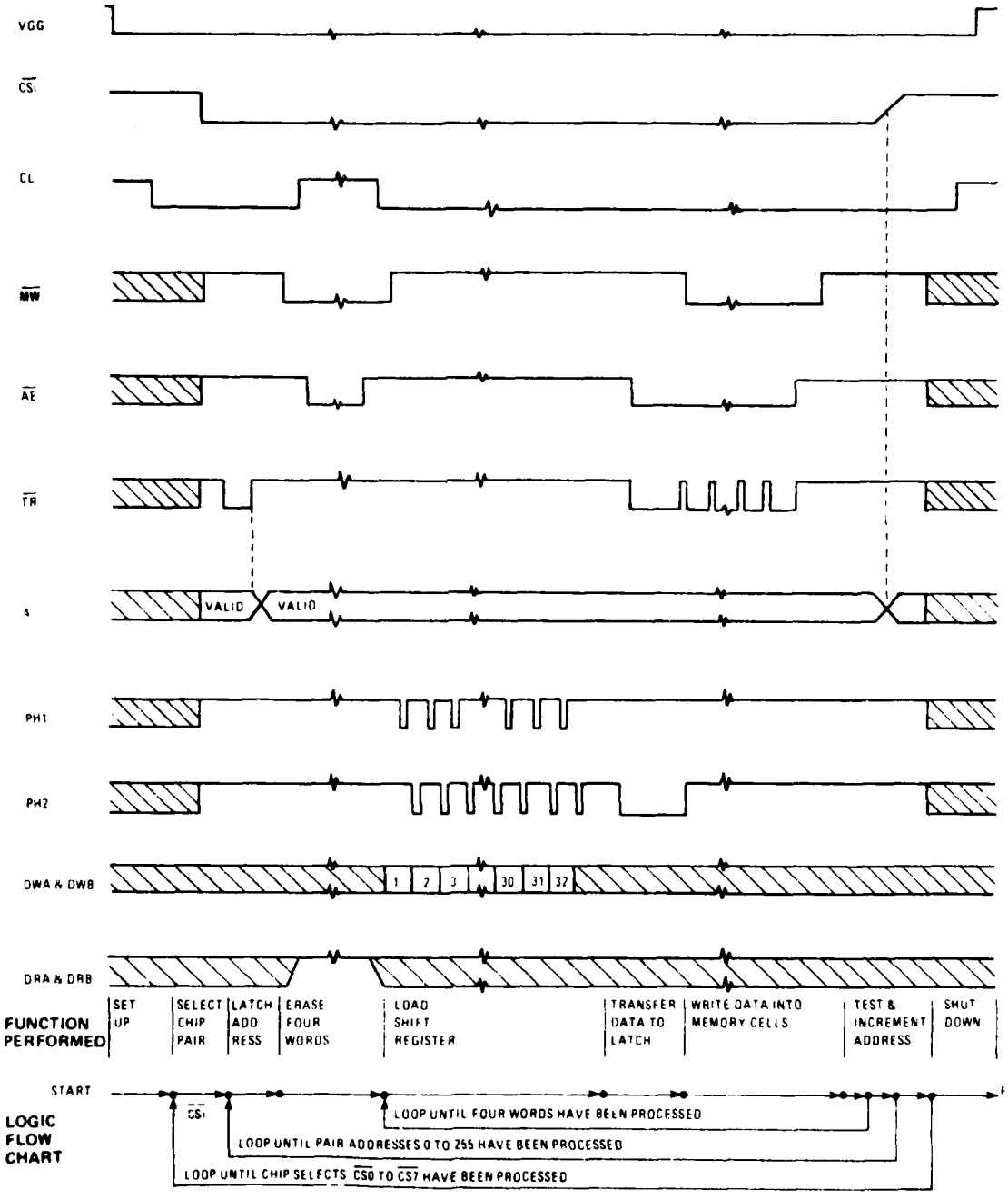
Event Sequence to Read Data from All Cells of a Hybrid Circuit



Event Sequence to Store Data in All Cells of a Hybrid Circuit Using Chip Erase



Event Sequence to Store Data in All Cells of a Hybrid Circuit Using Word Erase



BORAM 6008 Nonvolatile Integrated Circuit Block-Oriented Random-Access Memory Chip

Hybrid Circuit DC Electrical Parameters

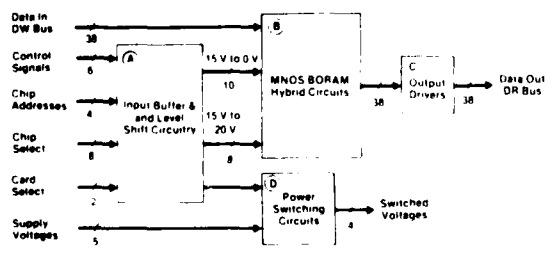
ELECTRICAL TEST PARAMETER	PARAMETER VALUE									UNITS
	55°C			25°C			125°C			
	min	typ	max	min	typ	max	min	typ	max	
INPUT TERMINAL LEAKAGE (Vin 5 V)		0 01	20		0 01	20		0 05	20	μA
CHIP SELECT LEAKAGE (Vin 22 5 V)		0 2	40		0 1	40		1	40	μA
OUTPUT TRISTATE LEAKAGE LOW (Vout 5 V)		0 2	10		0 1	10		0 2	10	μA
OUTPUT TRISTATE LEAKAGE HIGH (Vout +15V)		0 2	10		0 1	10		0 2	10	μA
OUTPUT VOLTAGE LOW (Iout +5 mA)		1 6	2 5		2 2	3 2		3 0	4 0	V
OUTPUT VOLTAGE HIGH (Iout - 5 mA)	13 0	13 8		12 5	13 5		12 0	13 0		V
SUPPLY CURRENT DESELECT STANDBY		3 0	40		2 0	40		6 0	40	μA
SUPPLY CURRENT SELECTED STANDBY		26	35		20	28		14	20	mA
SUPPLY CURRENT READ STATE		66	110		48	70		33	55	mA
SUPPLY CURRENT WRITE STATE ($\overline{TR}$ HIGH)		50	70		37	52		27	40	mA
SUPPLY CURRENT WRITE STATE ($\overline{TR}$ LOW)		26	36		20	28		14	20	mA
SUPPLY CURRENT CHIP ERASE STATE		26	36		20	28		14	20	mA
SUPPLY CURRENT WORD ERASE STATE		26	36		20	28		14	20	mA

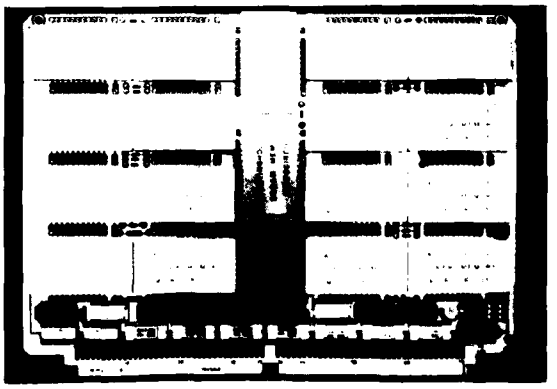
Power Dissipation

The nonvolatility of MNOS BORAM is exploited by employing power switching. The hybrid circuit should be turned on only during data transactions. Power analysis thus involves consideration of duty cycles. Even during the period of time that the hybrid is energized it is switched through operating states which have varied levels of power dissipation.

A typical operating sequence will result in an average power per hybrid circuit of about 750 milliwatts, or 375 milliwatts for each of the two active chips in the hybrid. Dissipation in the active mode is a function of temperature. As the temperature rises to 125°C the power will drop to about 600 milliwatts. If the temperature is reduced to −55°C, the power will increase to about 1.0 watt.

Typical Memory Card Organization





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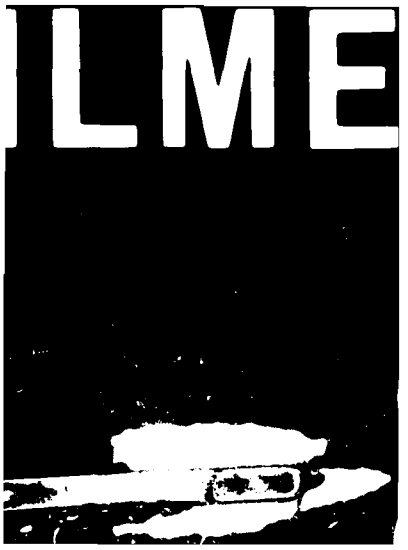
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